IM263

Low Power RF transceiver for narrow-band systems (ISM Radio Applications)

PRELIMINARY

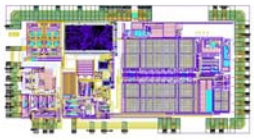
DATA SHEET

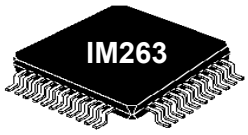
Typical Applications

- Narrow-band low power UHF wireless data transceiver
- 433 / 868 / 915 MHz ISM band systems
- Wireless alarm and security system
- Home automation
- Low power telemetry
- Remote control

Features

- Fully monolithic integrated SRD transceiver for ISM Band
- Multiband Transceiver : 433MHz, 868MHz, 915MHz
- No external RF components, integrated IF Filter
- Tuning step down to 10kHz
- Data rate up to 20 kbps
- High Sensitivity: –120dBm at 20kbps
- π/4 DQPSK data modulation/demodulation supported
- High immunity to interferers: Frequency-Hoping Spread Spectrum method supported
- Digital RSSI and carrier sense indicator
- Real-time programmable frequency and Automatic Frequency Control (AFC) make crystal temperature drift compensation possible without TCXO
- Full operating control via SPI bus (data-rate, modes, output power and modulation type)
- Integrated PLL and VCO
- Low current consumption
- Supply voltage: 2.7 to 3.3V
- Technology : SiGe BiCmos 0,35µm





Plastic QFP

Product Description

IM263 is a fully integrated transceiver designed for low power wireless application and for secured radio communications. It operates in the license-free ISM band :433MHz and 868-870 MHz in most European countries and 902-928 MHz in United States. IM263 is based on a half duplex bi-directional communication, especially suited for narrow band systems and complying with EN 300 220 . It includes an I-Q architecture receiver to reduce Antenna filtering constraint and require no external RF components .
Main operating parameters are programmed by a serial SPI interface making the IM263 an easy –to-use transceiver.

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1 Product Overview

1.1 *Functional description*

IM263 is a fully 44 pin IC transceiver optimised for licence-free ISM band operations from 433 MHz to 915 MHz, requiring very few external components.
The data exchange mode is half duplex. The device includes a dual conversion receiver (dual I/Q chain) to reduce antenna filtering constraint. It supports digital PHASE modulation and demodulation techniques with multi-channel capabilities.
An on-chip high frequency local oscillator based on a fully-embedded internal frequency synthesizer only requires an external low-cost crystal.
The receiving path includes a LNA, two down-converter mixers and a second internal local oscillator that provides the first frequency image rejection at once as well as integrated filters. All gain stages are level controlled, to achieve the best sensitivity (-120 dBm typical) in reception while avoiding front-end saturation with a tuning channel down to 10KHz. The gain is auto controlled and two external ceramic filters perform the base-band filtering.
User can choose adequate base-band bandwidth and fix maximum gain sensitivity of the ISM transceiver.
The device includes two serial control interfaces to configure the power management and the channel selection, allowing a very-fast tuning time.

1.2 *Functional bloc diagram*

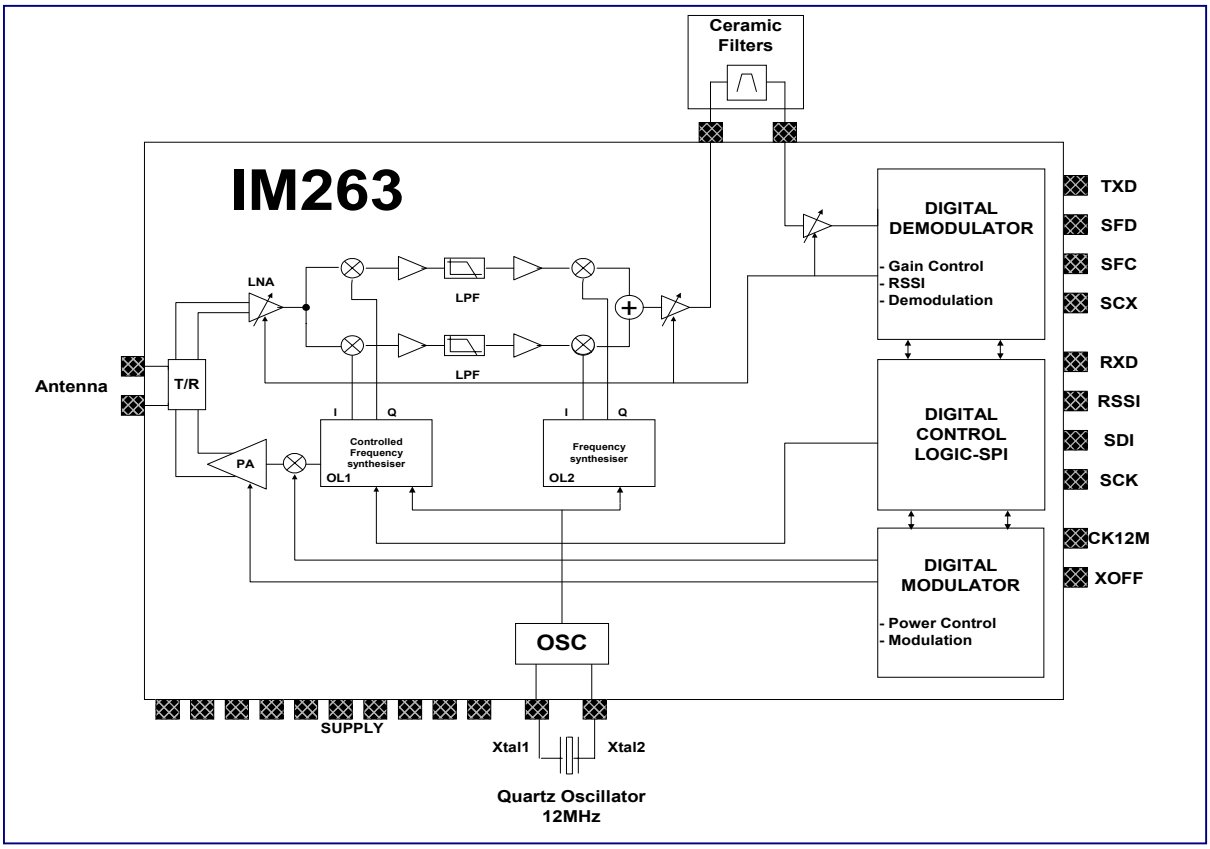

Fig. 1 : Simplified block diagram

1.3 *Pin description*

Abbreviations:

DIH : Digital CMOS input with pull-up ;
DCI : Digital CMOS Input;
DCIT : Digital CMOS Input with Schmitt trigger;
DCO : Digital CMOS Output;

AIO : Analog Input/Output;
AI : Analog Input;
AIO : Analog Output;

Nb	Name	I/O type	Description	Polarity
	VCCA1	-	Analog Supply voltage #1	-
	VCCA2	-	Analog Supply voltage #2	-
	VCCA3	-	Analog Supply voltage #3	-
	VCCA4	-	Analog Supply voltage #4	-
	VCCA5	-	Analog Supply voltage #5	-
	VCCA6	-	Analog Supply voltage #6	-
	VCCA7	-	Analog Supply voltage #7	-
	VCCA8	-	Analog Supply voltage #8	-
	GNDA1	-	Analog Ground #1	-
	GNDA2	-	Analog Ground #2	-
	GNDA3	-	Analog Ground #3	-
	GNDA4	-	Analog Ground #4	-
	GNDA5	-	Analog Ground #5	-
	GNDA6	-	Analog Ground #6	-
	GNDA7	-	Analog Ground #7	-
	VDD	-	Digital Supply voltage	-
	GND	-	Digital Ground	-
	VCCP	-	Power Amplifier Supply voltage	-
	GNDP	-	Power Amplifier Ground	-
	RESETB	DCIODH	Hard Reset I/O	L
	RXANTP	AI	Antenna RF inputs/Outputs differential pair	-
	RXANTN	AI		-
	TXANTP	AO		-
	TXANTN	AO		-
	GC2U	AI	LNA Gain Control Input Current	-
	VCA	AO	AGCTime Constant Control	-
	OUTAGC	AO	AGC to LNA Feedback Control	-
	FILT11EXT	AIO	[Optionnal] Interface signal of the external PLL11 filter	-
	FILT12	AO	Output Interface signal of the external PLL12 filter	-
	VCTRL12	AI	Input Interface Signal of the external PLL12 filter	-
	CFI1P	AO	Ceramic filter #1P driving signal	-
	CFI1N	AO	Ceramic filter #1N driving signal	-
	CFO1P	AI	Return signal from ceramic filter #1P	-
	CFO1N	AI	Return signal from ceramic filter #1N	-
	CFI2	AO	Ceramic filter #2 driving signal	-
	CFO2	AI	Return signal from ceramic filter #2	-
	XTALI	AIO	Crystal oscillator interface signals	-
	XTALO	AIO		-
	CK12M	DCO	12 Mhz output clock	
	XOFF	DILT	Crystal driver deactivation	H
	RTX	DCIOH	Transmission/Reception data line	-

Nb	Name	I/O type	Description	Polarity
	SCX	DCO	RXD/TXD synchronization signal	H
	SDIO	DCIOL	Main configuration interface serial data in/out	-
	SCK	DCIT	Main configuration interface serial clock in	–
	DNC	-	Do not Connect	–

1.4 Package outline: PQFP44

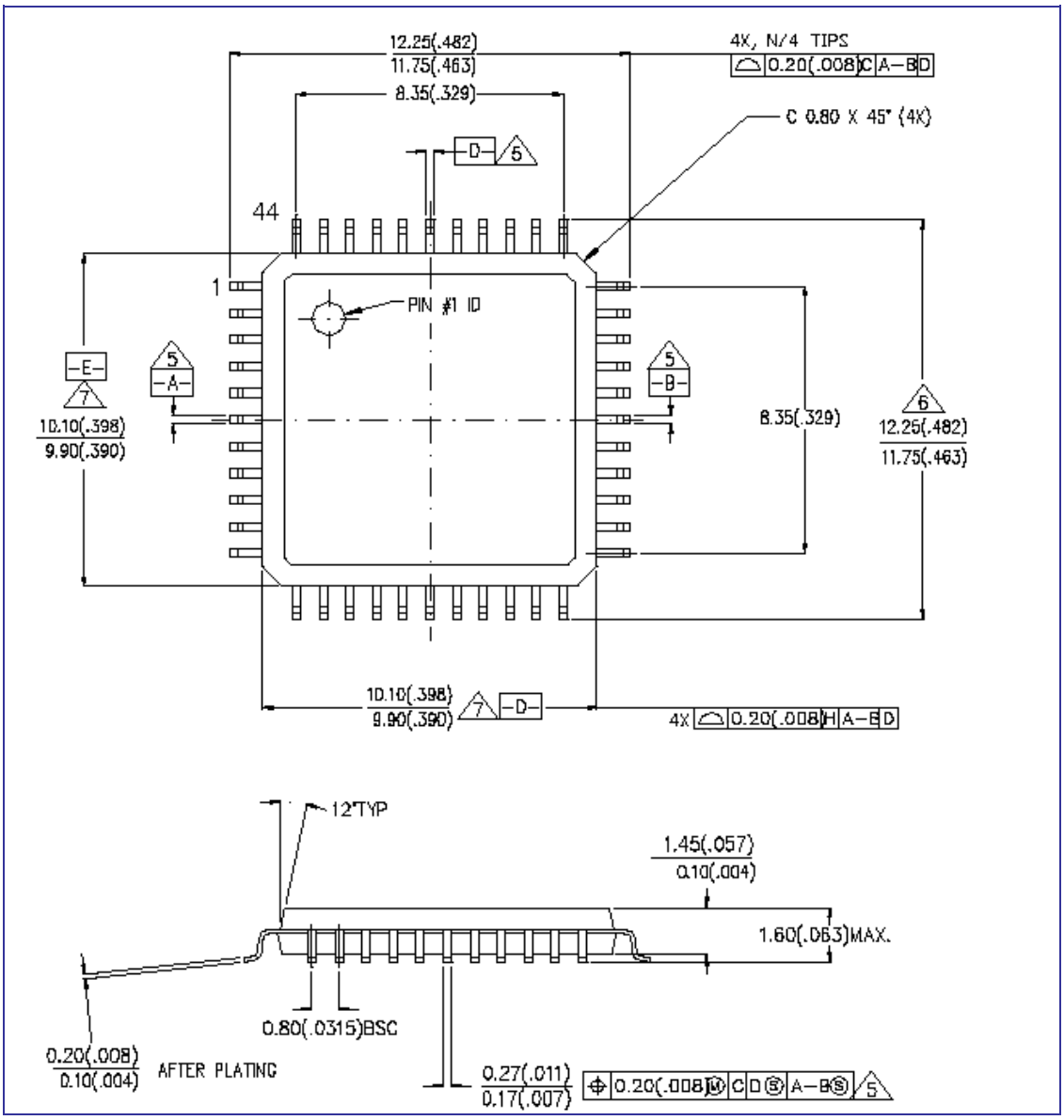

Fig. 2 : Outline drawing

2 Product Configuration

2.1 *SPI and MAIN CONFIGURATION INTERFACE*

2.1.1 SPI Interface

The circuit is configured via a simple 2-wire SPI-compatible interface (SDIO, SCK).
The control structure is made on a byte wise basis : configuration registers are 8-bits wide.
A 7-bits address pointer and a Read/Write control flag are is specified on any access.

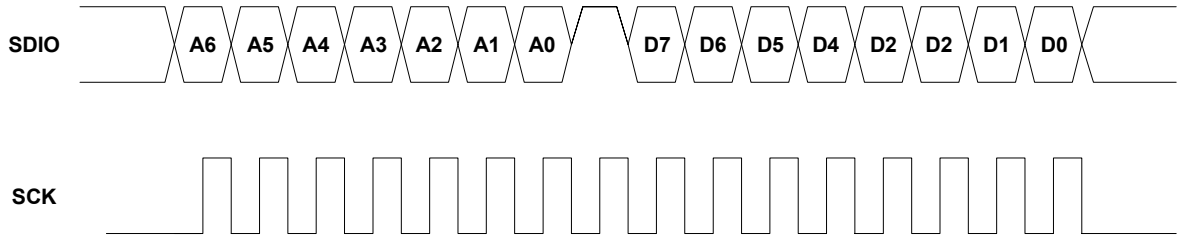

Figure 1 - SPI timing diagram : Write Access

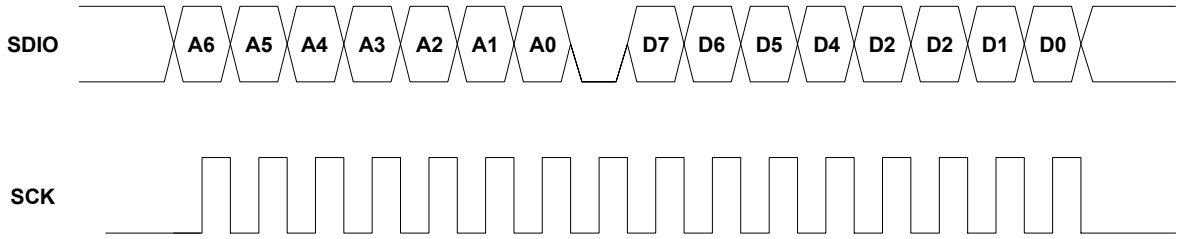

Figure 2 - SPI timing diagram : Read Access

The input address and data bits are sampled on the rising edge of the serial clock SCK.
Exactly 16 bits are exchanged between the circuit and its host for any Read of Write access.

Frames are composed consecutively by a 7-bits address field A[6:0], a Read/Write Flag and a data byte D[7:0].
A Read/Write flag positioned at a LOW level indicates a Read access.
For Read access, the flag must be set in a high impedance state : the internal pull-down resistor connected to SDIO will insure a LOW level on the line.

The address field and the Read/Write Flag are always driven by the Host.
The data field is issued by the host during Write access.
During Read access, the data bits are issued by the circuit on the falling edges of SCK. The data bits should be sampled by the host on the rising edges of the serial clock.

The most significant bits are transmitted first.

The 12-MHz main device clock must be running during operations.
On reception of a Write/Programming frame, the SPI interface stores the data received into the register pointed by the address specified.
A minimum guard delay is required between consecutive Write programming frames. This delay is measured between the last rising edge of a frame and the first one of the next frame.
No guard delay is required between a Read frame and a Write frame.

Characteristics	Min
SCK minimum High/Low pulse width	10 ns
SDIO in to SCK rising edge setup time	10 ns
SCK rising edge to SDIO hold time	10 ns
Consecutive Write frames Guard delay	300 ns

Table 1 - timings specifications

2.1.2 Memory-space organization

Internal Address	Name	Function
00	MAIN	Main operating mode control Register
01	COMCONF1	Digital Communications mode control Register
02	COMCONF2	Digital Communications mode control Register
03	TPHIS	HF mixer sinus input test register
04	TPHIC	HF mixer cosine input test register
05	TSEL	Test control Register
06	HF11E	ISM band Selection Register
07	HF12E(MSB)	HF Frequency Configuration Registers
08	HF12E(LSB)	
09	HF12D	HF Frequency Incrementation/Decrementation command.
0A	PAGC	Power Amplifier Gain Control Register
0B	ACONF	Analog configuration register
0C	DECR	Bit Demodulator/Decoder Configuration Register
0D	RSSI	Received Signal Strength Indicator Register
0E	DCOIN	Demodulator Digital oscillator input
0F	PHIIN	Demodulated phase
others	*Reserved (illegal access)*	

Table 2 - Memory-space organization

2.1.3 Registers

MAIN : Main control Register

Register MAIN selects the operating mode of the main units of the device.

7	6	5	4	3	2	1	0
-	-	**-**	**ATXON**	**ARXON**	**PLLON**	**DMODE**	

DMODE – Defines the digital modem operating mode.
The direction of the bidirectional pin RTX is automatically set in accordance ([1]).
This field controls the activity of the digital units only.

- 00 : (Reception) Idle mode
- 11 : (Transmission) Idle mode.
- 01 : Reception mode.
- 10 : Transmission mode (Modulation ON).

PLLON – Activates the internal HF synthesizer

- 1 : ON.
- 0 : OFF.

ARXON – Activates the Analog Reception units

- 1 : ON.
- 0 : OFF.

ATXON – Activates the Analog Transmission units (HF mixer and Power Amplifier).

- 1 : ON.
- 0 : OFF.

Both ARXON and ATXON can NOT be set to "1" simultaneously without permanent damages.

Initialization value on reset :	h00
Address :	00
Access Mode :	R/W

1See also test register TSEL on page 13.

COMCONF1 & COMCONF2 : Digital Communications mode control Register

Registers **COMCONF1** and **COMCONF2** select or specifie the encoding characteristics of communications.

	7	6	5	4	3	2	1	0
COMCONF1	**PHINB [1:0]**		**SR[2:0]**			**U0**	**STYPE**	
COMCONF2	**LPDIS**	**GAMA[2:0]**			**PHISTEP [3:0]**			

STYPE - Defines the modulation type :

- 00 **:** Phase modulation.
- 01 : Frequency modulation.
- 1X : Reserved (test)

SR [2:0] - Defines the symbol rate according to the following formula :

$$SYMBOL\,RATE = \frac{2^{SR} \cdot F_{12M}}{38400}$$

SR	Symbol rate
0	0.313 ks/s
1	0.625 ks/s
2	1.25 ks/s
3	2.5 ks/s
4	5 ks/s
5	10 ks/s
6 (*)	20 ks/s (*)
7 (*)	40 ks/s (*)

(*) experimental

U0 - Enable symbols encoded with no modulation.

- 1 : Modulation OFF enabled.
- 0 : Disabled.

PHINB [1:0] - Specifies the total number of bit(s) (number of analog modulation levels) per symbol according to the following formula :

$$BITS/SYMBOL = 2^{PHINB}$$

Multi-level Frequency modulation is not supported : PHINB has to be set to “00” when the Frequency modulation type is specified (STYPE=01).
When the phase modulation type is specified, PHINB must be programmed in the range [0:2]: A maximum of 4 bits can be modulated per symbol.

PHISTEP [3:0] - specifies the minimum phase modulation depth according to the following formula :

$$MIN\,PHASE\,DEPTH = PHISTEP \times \frac{\pi}{8}$$

GAMA [2:0] – Specifies the symbol synchronization latency.

Initialization value on reset :	h00
Address :	01 & 02
Access Mode :	R/W

DECR : Bit Decoder/Demodulator Configuration Register

Controls the various parameters of the digital demodulator.

7	6	5	4	3	2	1	0
APB			**BETA**		**ALFA**		

APB : Specifies the cut-off frequency of the LOW-PASS FILTER at the output of the Phase detector of the Demodulation unit.
BETA :.DPLL Loop filter Cut-off frequency control.
ALFA : DPLL Loop filter Gain control.

Initialization value on reset : h00

Address :	0C
Access Mode :	Read/Write

TPHIS & TPHIC : HF mixer test register (for test purpose only)

Programmable input of the DACs.
The content of these registers are taken into account only when the field *STYPE* of register *COMCONF1* is set to "10".

	7	6	5	4	3	2	1	0
TPHIS	-	-	-	**TPHIS [4:0]**				
TPHIC	-	-	-	**TPHIC [4:0]**				

When the field *STYPE* of register *COMCONF1* is set to "10", the signal transmitted through the antenna has the following format :

$$\cos\left(\frac{\pi}{16}\cdot \mathrm{TPHIC}\right)\times\sin(\omega_c t)+\sin\left(\frac{\pi}{16}\cdot \mathrm{TPHIS}\right)\times\cos(\omega_c t)$$

TPHIS and TPHIC are considered as signed numbers.

Initialization value on reset :	h00
Address :	03 & 04
Access Mode :	R/W

RSSI : Received Signal Strength Indicator Register

	7	6	5	4	3	2	1	0
	-	-	-	-	**RSSI [3:0]**			

Initialization value on reset :	NA
Address :	0D
Access Mode :	Read Only

DCOIN : Demodulator Digital oscillator input

7	6	5	4	3	2	1	0
DCOIN[7:0]							

Initialization value on reset :	h00
Address :	0E
Access Mode :	Read Only

PHIIN : Detected phase from demodulator unit

7	6	5	4	3	2	1	0
PHIIN[7:0]							

Initialization value on reset :	h00
Address :	0F
Access Mode :	Read Only

TSEL : Test control Register

7	6	5	4	3	2	1	0
-	**-**	-	**DBROFF**	**TESTFI**	**RXSEL [2:0]**		

RXSEL [2:0] Controls the output test multiplexer on pins RTX and SCX.
The bidirectional pin RTX is forced in output mode when this field is different from 000.

RXSEL	RTX	SCX
000	Standard operating RX signal	Standard operating SCX signal
001	Output of the reception trigger (Input of the demodulation unit), after synchonization and debouncing (if enabled).	Output of the digital demodulator DCO.
010	NRZPHI[1]	NRZPHI[0]
101	Internal digital output I of the 600kHz oscillator	Internal digital output Q of the 600kHz oscillator
110	CKDIV12D1, divided output #1 of PLL12 VCO	CKDIV12D2, divided output #2 of PLL12 VCO
111	CKREF12, Reference clock of PLL12	ISINE12 : Quadrature state of the HF PLL12 (1: I=sinus & Q=cos)
100	CKDIV11, divided output of PLL11 VCO	ISINE11 : Quadrature state of the HF PLL11 (1: I=sinus & Q=cos)
others	*reserved*	

TESTFI : Reception Analog Filters debug Enable control bit.

DBROFF : Digital Demodulator Input debouncer Disable bit.

Initialization value on reset :	h00
Address :	05
Access Mode :	R/W

HF11E : ISM band Selection Register

Register HF11E selects the ISM band for communications.

7	6	5	4	3	2	1	0
-	-	-	-	-	**HFSTEP**	**HF11 [1:0]**	

HF11 [1:0] :
This field controls the frequency divider of the HF PLL11.

- 00 : 434Mhz band
- 01 : *Reserved*
- 10 : 868MHz band
- 11 : 915MHz ISM band

HFSTEP : Configure the minimum frequency step (experimental feature)

- 1 : 5 kHz.
- 0 : 10 kHz.

Initialization value on reset :	h00
Address :	06
Access Mode :	R/W

HF12E : HF Frequency configuration Registers (MSB & LSB)

	7	6	5	4	3	2	1	0
HF12E (MSB) :	-	-	-	-		**HF12E [10:8]**		
HF12E (LSB) :	**HF12E [7:0]**							

Initialization value on reset :	h00
Address :	07 & 08
Access Mode :	R/W

HF12D : HF Frequency Incrementation/Decrementation command register

7	6	5	4	3	2	1	0
-	-	**HF12D [5:0]**					

On any write access at the address of the HF12D register, the HF12 D value, considered as a signed number, is added to the HF12E register.

Initialization value on reset :	NA
Address :	09
Access Mode :	Write Only

The HF frequency can be configured, within a predefined ISM band, with a frequency step of 10kHz (when HFSTEP='0').
The ISM band is selected by register HF11. The HF12E register selects the lowest part of the HF Carrier frequency. The allowed programming range for HF12E is defined in Table 3.

The relation between reception/transmission central frequency and both HF11[1:0] and HF12E[9:0] control fields is defined as :

$$HF\,CARRIER\,FREQ=\left(D_{11}+\frac{HF12E}{1200\times 2^{HFSTEP}}\right)\times F_{12M}\quad(+5\,kHz\ in\,receive\,mode),$$

where :

- D11 is a constant depending on the selected ISM band : See Table 3.
- F_{12M} is the frequency of the crystal oscillator, i.e. 12.0 Mhz.
- HF12E is considered as an unsigned (positive) number.

HF11	ISM Band	Operating Frequency range	D11	HF12E Allowed programming range	
				HFSTEP=0	HFSTEP=1
00	434Mhz	433.05 - 434.79	36	105 - 279	210 - 558
10	868 MHz	868.00 - 870.00	72	400 - 600	800 - 1200
11	915MHz	913.10 - 918.00	76	110 - 600	220 - 1200

Table 3 - HF Frequency operating ranges

PAGC : Power amplifier Attenuation control register

Controls the gain of the transceiver antenna power amplifier

7	6	5	4	3	2	1	0
-	-	-	-	PAGC [3:0]			

Initialization value on reset : h00

Address : 0A

Access Mode : Read/Write

The relationship between the content of this register and the output power is defined as :

$$OUTPUT\,POWER=\frac{15.0-PAGC}{15.0}\times POWER_{MAX}\text{ , where :}$$

- PAGC is considered as a *positive unsigned* number.
- $POWER_{MAX}$ is the maximum output power deliverable at the output of the power amplifier.

ACONF : Analog configuration register

7	6	5	4	3	2	1	0
F11EXT	**INVIQ600K**	**AOAMP[2:0]**			**AOBUC[2:0]**		

AOAMP[2:0] : Controls the gain of various amplifiers of the reception channel.
Recommended configuration : TBD

AOBUC[2:0] : Controls the gain of various amplifiers of the reception channel.
Recommended configuration : TBD

INVIQ600K : controls the quadrature of the 600kHz internal oscillator.
Recommended configuration : TBD

F11EXT : Specifies the PLL11 loop filter type.
1 -**1 :** specifies to use an external filter on the IO pin FILT11EXT.
2 -**0:** Use the internal filter (The IO pin FILT11EXT must be left unconnected)

Initialization value on reset :	h00
Address :	??
Access Mode :	Read/Write

2.2 SIGNAL INTERFACE

In both transmission and reception modes, data bitstreams are exchanged between the circuit and its host via a simple 2-wires interface : RTX , SCX.

Data are exchanged on the RTX line, synchronized by the SCX signal provided by the circuit according to the following protocol :
In transmit mode RTX is used as data input by the circuit.
Data bits are clocked into the modulator at the falling edge of SCX.
In receive mode the circuit does the bit-level synchronization.
It provides received data at RTX, synchronized by the SCX signal.
The data may be clocked into the interfacing circuit at either the rising or the falling edge of SCX.

The total number of bits exchanged during a modulation-symbol period depends on the configuration of the device.
As long as the device is in transmit mode with modulation disabled (see field DMODE in register **MAIN** on page 9), no transfers are initiated by the CIRCUIT on the RTX line.
In the other case, when the device is either in reception mode or in transmission mode (with modulation enabled), exactly $NB=U0+2^{PHINB}$ bits (see register **COMCONF2** on page 10) are consecutively exchanged, every symbol period, between the CIRCUIT and the Host.
The word composed by these bits is called SYMWORD[NB-1:0] is the next sections.

If the control bit U0 in register **COMCONF2** is set to “1”, the first bit transferred (b[NB-1]) has the following function :

- In transmission mode, a LOW level disables analog modulation for the next symbol. The other bits are not taken into account (but have to be sent by the host).
- In reception mode, a LOW level indicates that no modulation was detected in the last symbol. The other bits are all forced to '1' or '0', as if the U0 bit was not set [2].

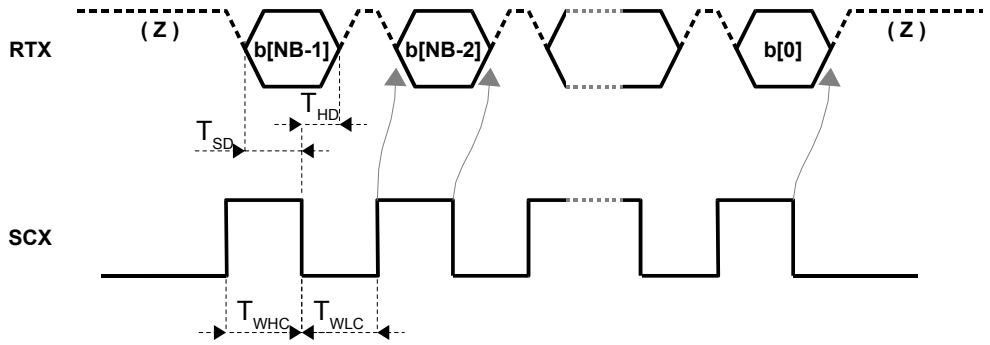

Figure 3 - Transmit Mode Signal Interface timing diagram

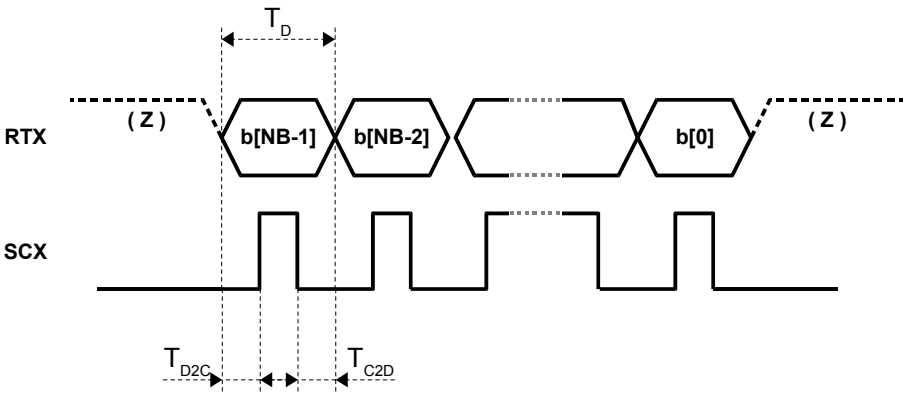

Figure 4 - Receive Mode Signal Interface timing diagram

Parameter	Symbol	Min	Max
SCX Positive pulse width in transmit mode	T_{WHC}	$8\times T_{12M}$	-
SCX Negative pulse width in transmit mode	T_{WLC}	$8\times T_{12M}$	-
RTX to SCX setup time in transmit mode	T_{SD}	10 ns	-
SCX to RTX hold time in transmit mode	T_{HD}	0 ns	-
RTX bit width in receive mode	T_D	$16\times T_{12M}$	-
RTX to rising SCX delay in receive mode	T_{D2C}	$4\times T_{12M}$	-
RTX to falling SCX delay in receive mode	T_{C2D}	$4\times T_{12M}$	-

Table 4 - Signal Interface Timing Specifications

2This feature enables the host to correct the demodulated value when an absence of modulation is not allowed by the higher-level protocol at certain positions of the symbol streaming.

2.3 FREQUENCY AND PHASE MODULATIONS

2.3.1 Phase Modulation

2.3.1.1 General rules

Modulation	SYM= SYMWORD [2^{PHINB}-1 : 0]	Phase modulation
Modulation OFF	-	$\Phi(t)=0$
Modulation ON	< 0	$\Phi(t)=(1+SYM)\times PHISTEP\times\frac{\pi}{8}\times \sin(\omega_{SYM}t)$
	≥ 0	$\Phi(t)= SYM\times PHISTEP\times\frac{\pi}{8}\times \sin(\omega_{SYM}t)$

2.3.1.2 PHINB=0

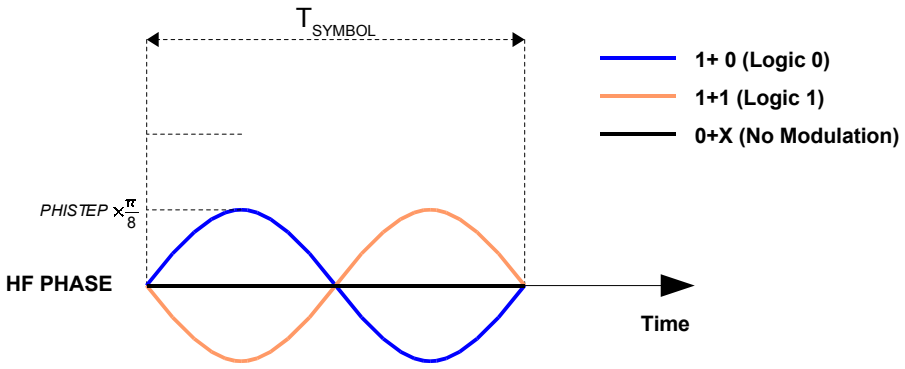

Figure 5 - symbol coding using phase modulation for PHINB=0

2.3.1.3 PHINB=1

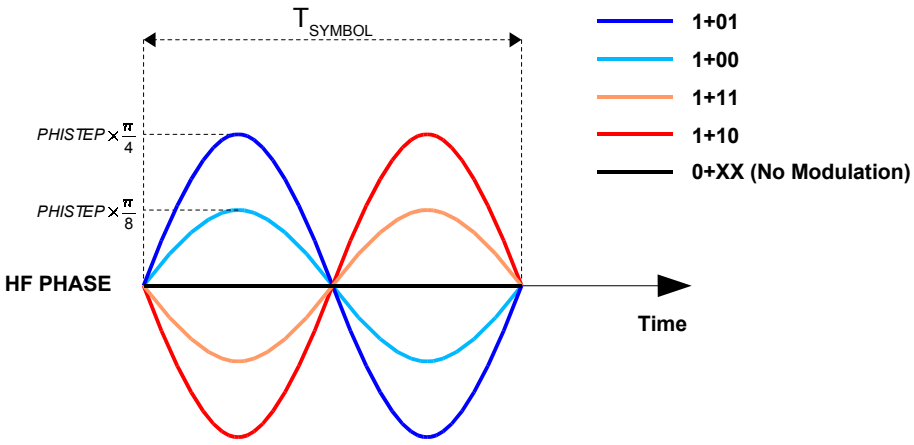

Figure 6 - symbol coding using phase modulation for PHINB=1

2.3.2 Frequency Modulation

2.3.2.1 PHINB=0

The following sequences are defined:

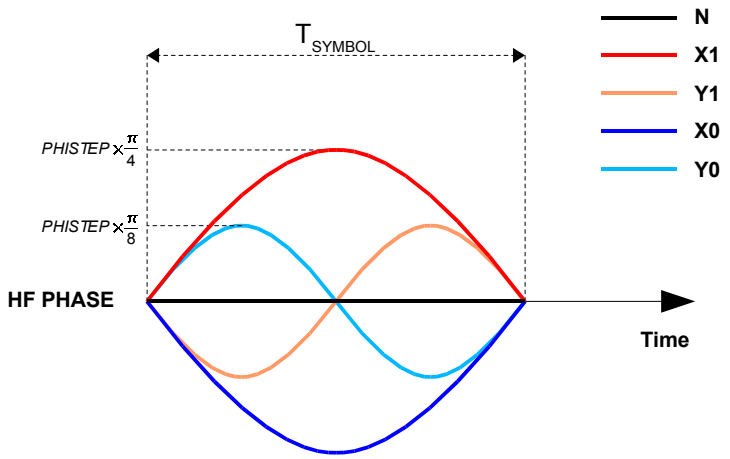

Figure 7 - symbols coding using Frequency modulation for PHINB=0

The above sequences are used to code the following information :

Logic 1	1+1	1	Sequence X1 with the following exception : If there are two or more contiguous 1's, sequence Y1 shall be used from the second 1 on.
Logic 0	1+0	0	Sequence X0 with the following exception : If there are two or more contiguous 0's, sequence Y0 shall be used from the second 0 on.
No Modulation	0+X	-	Sequence N.

2.3.2.2 PHINB>0

Multi-level Frequency modulation is not supported.

2.4 POWER-ON-RESET

A Power-on Reset pulse is generated on-chip when V_{DD} rise is detected.
It eliminates external RC components usually needed to create a Power-on Reset.
When the device exits the reset condition, device operating parameters (voltage, frequency, temperature, etc) must be met to ensure operation.
At the end of the power-on-reset sequence the device starts immediately measurements, and is ready to receive programming frames though its host interface.
The digital bidirectional port RESETB can be employed to reset devices on the same PCB as the circuit, or to force asynchronous reset of the circuit at any time :
The default inactive level of this signal is high. The terminal is pulled-up by an internal resistor connected to VDD.
During the internal hard reset of the circuit, the port RESETB is forced to a low level by the device.
At any other instant, the Host may force this terminal to a low level, inducing a hard reset of the circuit.

3 Electrical characteristics

3.1 *Absolute maximum ratings*

Maximum ratings are the extreme limits to which the device can be exposed without permanent damages. It is not guaranteed to operate properly at the maximum ratings. Refer to next chapter for guaranteed conditions.

Parameter	Min	Max	Unit
Supply voltage	0	3,6	V
Storage temperature	-55	125	°C

Table 5 – Absolute maximum ratings

3.2 *Operating conditions*

Parameter	Min	Typ	Max	Unit
Operating free-air temperature	-20	27	+80	°C
Operating junction Temperature	-20	27	+90	°C
Supply voltage	2.7	3.0	3.3	V
Supply current in Receive mode		25		mA
Supply current in Transmit mode(1)	35			mA
Supply current Power down mode(2)		1.0		µA

(1): for 10mW E.R.P.
(2): Preliminary information.

Table 6 – Operating conditions

3.3 *AC Parameters*

(T_A = 25 °C, V_{CC} = 3 V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Operating Frequency Range	FR	-	433.05 - 434.79 868 - 870 913.1 - 918			MHz	1
Digital frequency tuning step	N	For all frequency range	-	10	-	kHz	
Channel Bandwidth	CBW	Fixed by ceramic filter 455 kHz Bandwidth	-	-	35	kHz	
Sensitivity	S_{RF}	BER = 1%, DR=5kbps, RF load = 50 Ω	-120	-	-	dBm	2,4
Co-Channel Rejection	CR	depending on 455 kHz ceramic filters used	-	-	-	dB	
Maximum Receiver Input Level	ILMAX	1 channel, BER = 1%		-15		dBm	4

Antenna Port Impedance	Z_A	433.92 MHz 869.00 MHz 915.00 MHz	-	50 50 50	-	Ω	4
Quartz oscillator frequency	F_{12M}			12.0		MHz	
Receiver Wake Up Time	t_{WR}	Cold Start		3		ms	4
RX to TX toggle time	t_t			1		ms	4
Time for RX recover normal function after saturation	t_{rec}			1		ms	4
Effective Radiated Power in (digital control)	ERP	Freq. range 433.05- 434.79 MHz 868.00 - 868.60 MHz 868.70 - 869.20 MHz 869.40 - 869.65 MHz 869.70 - 870.00 MHz			10 25 25 500 5	mW	3

Table 7 – AC parameters

Note (1): The ISM Band Transceiver is compliant to I-ETS 300-220.
Note (2): The calculation of the sensitivity takes only the modulated signal bandwidth into account.
Note (3): Non-specific Short Range Devices ERC/REC 70-03 E
Note (4): Preliminary informations

4 Application Notes

4.1 General principle

IM263 is tailored to provide both high integration and high-class sensitivity for a cost effective electronics. IM263 meets the *RF Plug & Play* concept, it requires no external RF devices and no RF tuning at board level. The amount of external components is drastically reduced. Moreover, IM263 enables the use of extremely low-cost external parts such as:

- Industry standard 455KHz ceramic filter
- 12 MHz standard crystal
- Standard R & C discrete parts

4.2 Typical application schematics

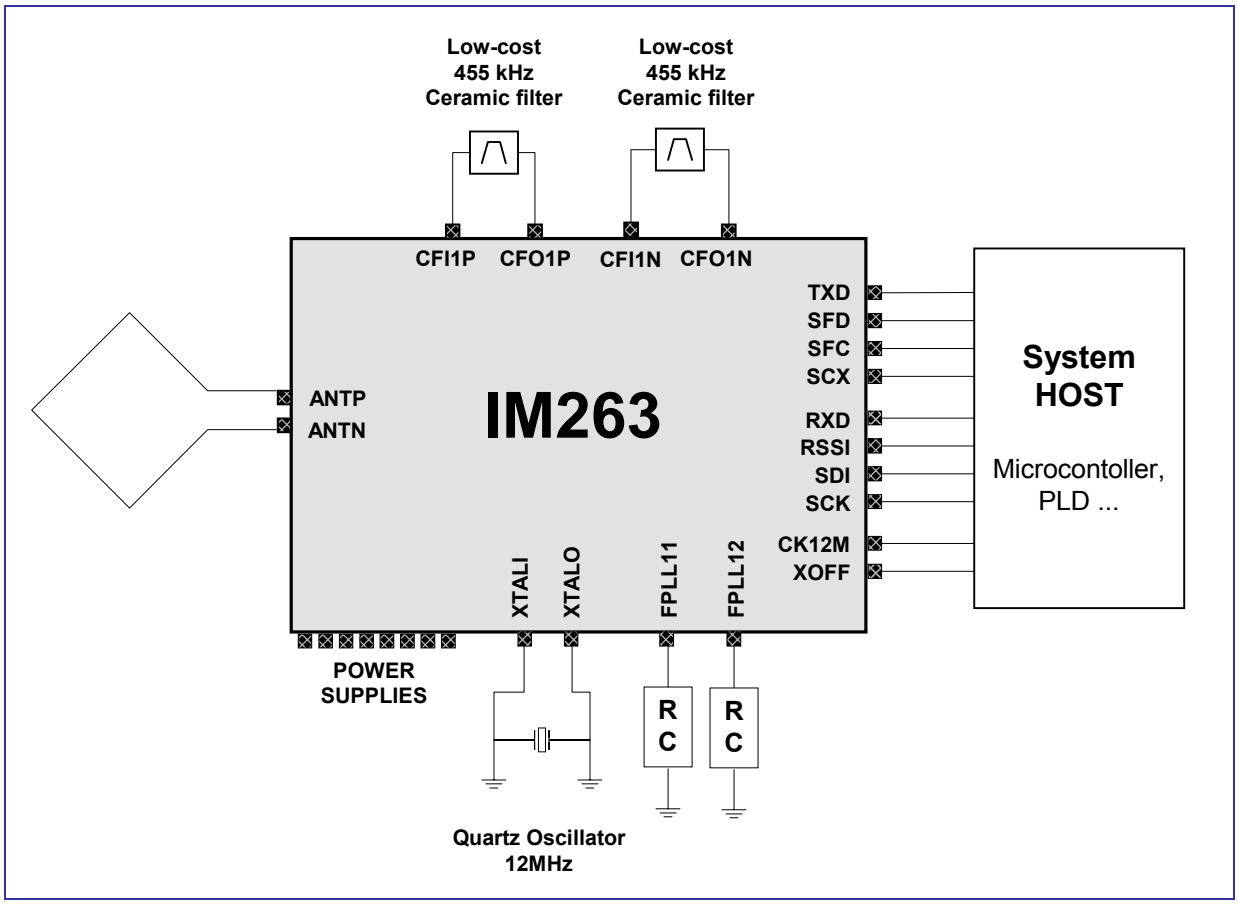

Fig. 3 : Application drawing

4.3 Software/digital application notes

To Be Defined

4.4 Quartz application note

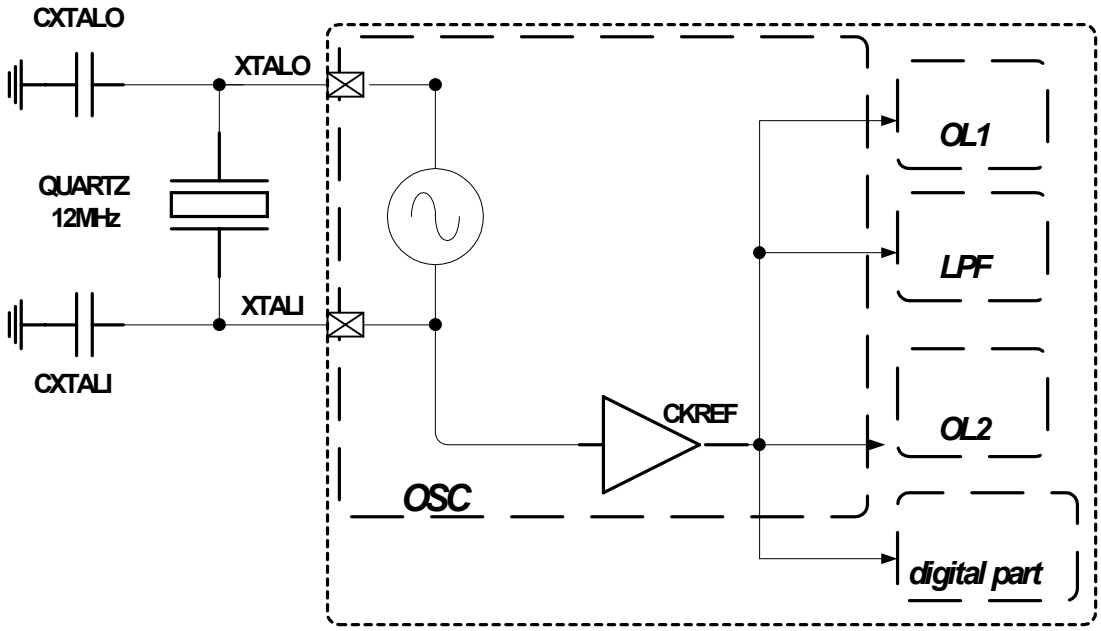

Figure 8 - Quartz typical application schematic

Component	Symbol	Value
Capacitor	CXTALO	10 pF
Capacitor	CXTALI	10 pF
Quartz	XTAL	12.0 Mhz 100 ppm max

Table 8 Recommended Components

4.5 HF PLL Filters application note

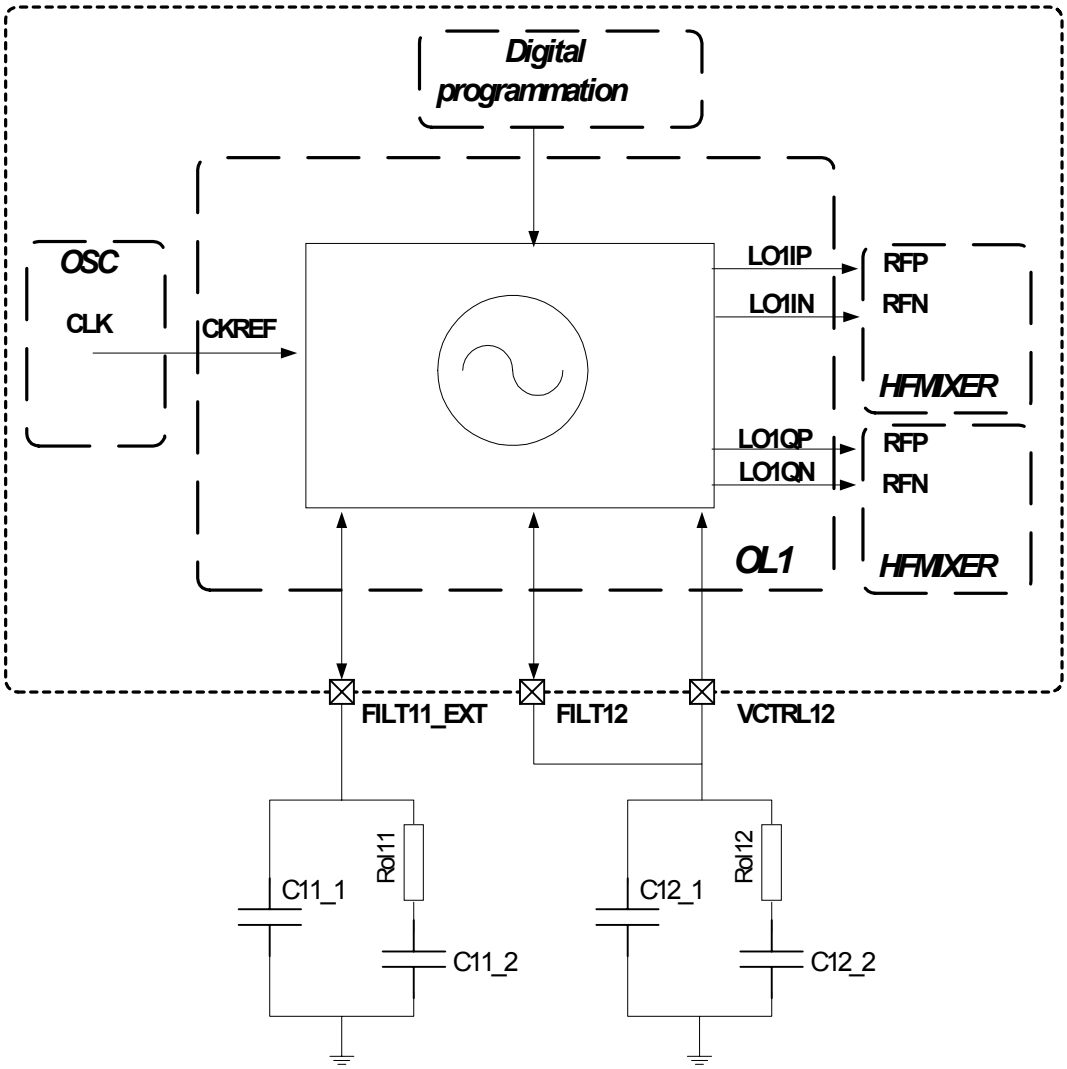

Figure 9 - PLL Filters typical application schematic

Component	Symbol	Value
Capacitor (optionnal)	C11_1	10 pF
Capacitor (optionnal)	C11_2	100 pF
Resistor (optionnal)	Rol11	22 kΩ
Capacitor	C12_1	2 nF
Capacitor	C12_2	20 nF
Resistor	Rol12	15 kΩ

Table 9 PLL Filters Recommended Components

Both filters must be connected as close as possible to the device package due to high noise sensitivity.

4.6 Reception Filters application note

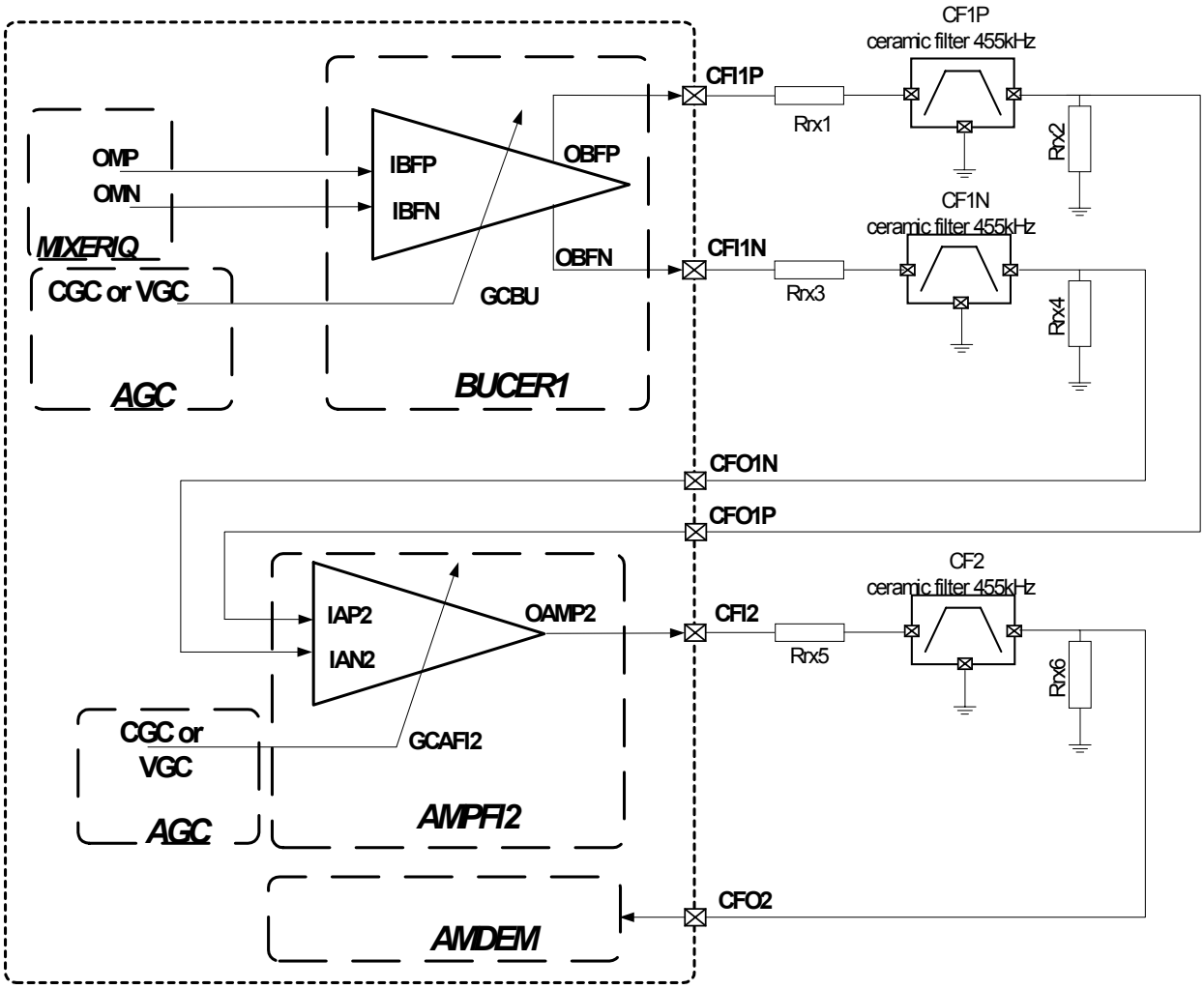

Figure 10 - Reception Filters typical application schematic

Component	Symbol	Value
Resistor	Rrx1	1 kΩ
Resistor	Rrx2	1 kΩ
Resistor	Rrx3	1 kΩ
Resistor	Rrx4	1 kΩ
Resistor	Rrx5	1 kΩ
Resistor	Rrx6	1 kΩ
455 kHz Ceramic Filter	CF1P	Example : Murata ref. CFUCF455KA2X-RO
	CF1N	
	CF2	

Table 10 Reception Filters Recommended Components

Filters must be connected as close as possible to the device package due to high noise sensitivity.

4.7 Antenna Adaptation

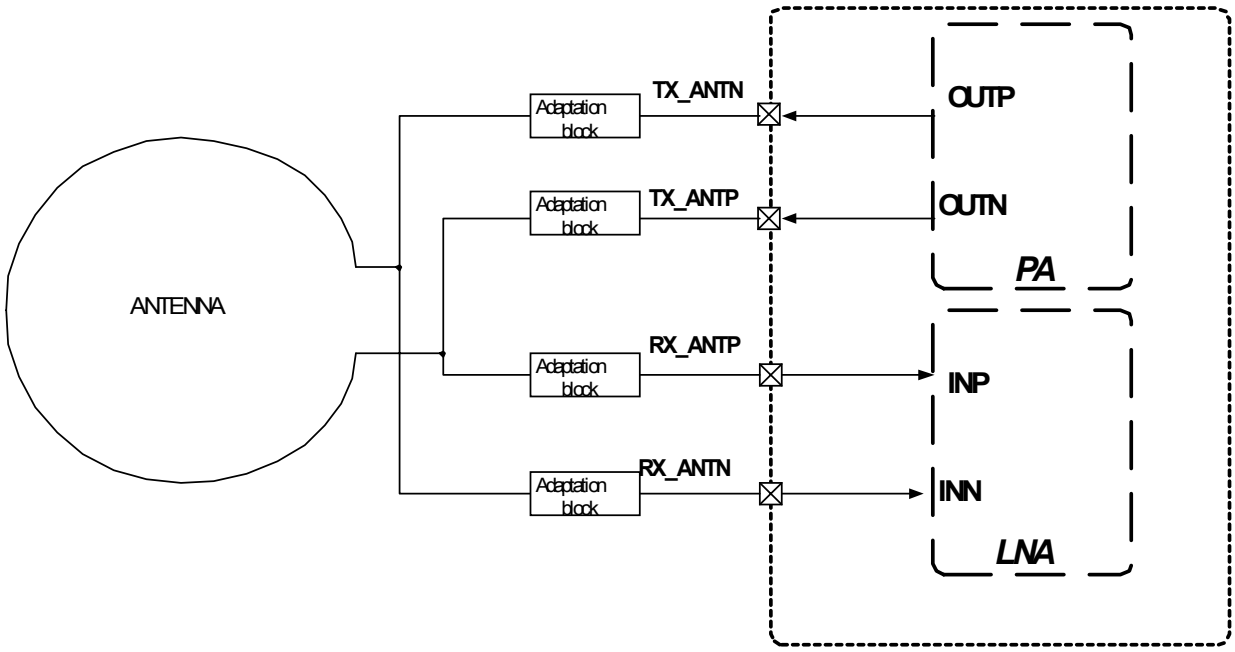

Figure 11 - Antenna Adaptation Principle

When the bit ARXON in register MAIN is unset (idle or Transmit mode), the inputs RX_ANTP and RX_ANTN are in high impedance state.

When the bit ATXON in register MAIN is unset (idle or Receive mode), the outputs TX_ANTP and TX_ANTN are in high impedance state.

5 Notes