

DATA SHEET

Typical Applications

- Central Office Equipment Applications
- PABX
- Keyphone Systems
- Remote Control Equipment
- Consumer Telephony Products

Features

- Single 5V or 3.3V Power Supply
- Detects All 16 Standard Digits
- Uses Inexpensive 3.58 MHz Crystal
- Provides Guard Time Controls to Improve Speech Immunity
- Output in 4-Bit Hexadecimal Code
- Build-In 50/60 Hz and Dial Tone Rejection
- Pin Compatible with SSI-204, MC145436 , MC14LC5436



Product Description

The circuit is a silicon gate CMOS device containing filters and decoder for detection of a pair of tones conforming to the DTMF standard with outputs in hexadecimal. Switched capacitor filter technology is used together with digital circuitry for the timing control and output circuits.

The circuit provides excellent power line noise and dial tone rejection and is suitable for applications in central office equipment, PBX, any key phone systems, remote control equipment and consumer telephony products.

Functional description

The SW136 monolithic DTMF receiver offers small size, low power consumption and high performance. It separates the high and low group tones from the dial up tone pair, verifies the frequencies and duration before passing the corresponding hexadecimal code to the output.

DTMF Frequency Coding

The telephone keypad matrix and its DTMF coding are shown. Column 4 is kept for special signaling and normally it is not available on telephone keypad but is accepted by the DTMF receiver.

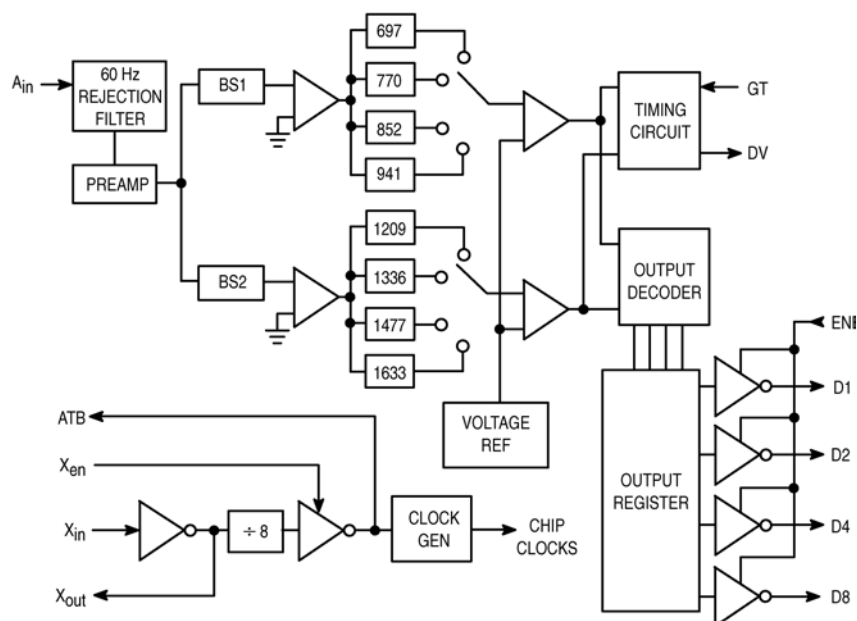
Column:	1	2	3	4	Row:
697	1	2	3	A	1
770	4	5	6	B	2
852	7	8	9	C	3
941	*	0	#	D	4
	1209	1336	1477	1633	
	DTMF High frequency (Hz)				

DTMF Hexadecimal Output Codes

Digit	Output Code			
	D8	D4	D2	D1
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
0	1	0	1	0
*	1	0	1	1
#	1	1	0	0
A	1	1	0	1
B	1	1	1	0
C	1	1	1	1
D	0	0	0	0

Table 1

Functional Diagram



AUDIO PREPROCESSOR

The Audio Preprocessor is an analog filter which band limits the input analog signal between 500 Hz and 3kHz. In addition, it emphasizes the 2 kHz to 3 kHz voice region. Band limiting suppresses supply noise, dial tone frequencies and high frequency noise. The emphasized voice region helps to equalize the audio response since many phone lines tend to roll off at about 1 kHz. In addition, preservation of the upper voice frequencies is important in providing speech immunity.

TONE BAND SPLITTING

After the analog signal is preprocessed, it is split into two bands, each of which contains only one DTMF tone group. The band split filters are actually band-stop filters to maintain all frequencies except the other tone group; this is done to maintain all analog information to enhance speech immunity but not allow other tone group to act as interfering noise for the band being detected. These band stop filters have “floors” that limit the amount of tone pair twist, which further enhances speech immunity.

ZERO-CROSSING DETECTORS

The output of each band-split filter is amplified and limited by a zero-crossing detector (limiter). The function of the zero-crossing detector is to produce a square wave at the prime frequency emanating from the band-split filter. If a pure tone is not present, as in the case of voice or other interfering noise, a rectangular wave with a variable period will result. Proportional to the interference, the limiter output power is spread over a broad frequency range as the zero-crossings “dither”. When a high level of noise or speech occurs, no single band-pass filter pair will contain significant power long enough to result in tone detection. On the other hand, when a pure DTMF tone exists with acceptable noise levels, the output of the limiter will not have any significant dither and tone detection will occur. The zero-crossing detector also acts as an AGC (Automatic Gain Control) in that the output amplitude is independent of input amplitude; this additionally establishes an acceptable signal-to-noise ratio not dependent on tone amplitude.

BANDPASS FILTERS & AMPLITUDE DETECTORS

The band-pass filters perform tone frequency discrimination. Their responses are tailored so that if the frequency of the limited square wave from the zero-crossing detector is within the tone frequency tolerance, the filter output will exceed the amplitude detector threshold. The amplitude detectors are interrogated periodically by the digital control circuitry to ascertain the presence of only one tone in each band for the required duration. In a similar fashion, valid pauses are measured by the absence of valid tone pairs for the specified time.

The digital part includes circuitry to check coincidence and duration of tone pairs, and to generate the filter clocks.

The coincidence and timing circuitry ensures that two and only two tones are present for sufficient duration to be decoded as a valid hit. The circuitry ensures that small gaps in a tone pair are not recognized as inter-digit intervals and that longer gaps are.

The clock generation circuit accepts as input a square wave from the crystal oscillator or from an external source. Further this input is divided by eight to generate the filter clock phases. To ensure that the clocks do not overlap each clock is high for a period of time less than a half of the period.

TIMING CIRCUIT

This unit has as inputs the outputs from the level detectors and GT input signal. The purpose of this block is to estimate whether the input pair signals satisfy the standard's requirements.

OUTPUT DECODER

This unit has to detect the valid DTMF pair of signals from the level detectors and to load it to the Output Register block.

OUTPUT REGISTER

This is the block where the decoded digit is loaded and kept until a new one is decoded or the block has been cleared. In order to have the decoded number at the output pins ENB signal should be set to active level.

CLOCK GENERATOR

This block has to provide the required frequencies used in the circuit. It receives square form waves from the crystal oscillator or other external source of frequency and divides it to 8 after which using counters the required frequencies are obtained.

Absolute Maximum Ratings

(Voltages Referenced to GND unless otherwise noted)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +6.0	V
Input Voltage, any pin Except A_{in}	V_{in}	-0.5 to $V_{DD}+0.5$	V
Input Voltage A_{in}	V_{in}	$V_{DD}-10$ to $V_{DD}+0.5$	V
DC Current Drain per Pin	I	± 10	mA
Power Dissipation	P_D	100	mW
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

Electrical AC Characteristics

($V_{DD}=5.0[V] \pm 10\%$; $T_A=-40$ to 85 °C) See Fig.1

Characteristics	Symbol	Min	Typ	Max	Unit	
Tone On Time	For Detection For Rejection	TONE _{on}	40	-	-	ms
			-	-	20	
Pause Time	For Detection For Rejection	TONE _{off}	40	-	-	ms
			-	-	20	
Detect Time	GT=0	t_{det}	22	-	40	ms
	GT=1		32	-	50	
Release Time	GT=0	t_{rel}	28	-	40	ms
	GT=1		18	-	30	
Data Setup Time	t_{su}	7	-	-	μ s	
Data Hold Time	t_h	4.2	4.6	5	ms	
Pulse Width	GT	$t_{W(GT)}$	18	-	-	μ s
DV Reset Lag Time	$t_{lag(DV)}$	-	-	5	ms	
ENB High to Output DV ($C_L=35pF R_L=500\Omega$)	t_{EHDV}	-	120	500	ns	
ENB Low to Output High-Z ($C_L=35pF R_L=500\Omega$)	t_{ELDZ}	-	110	300	ns	

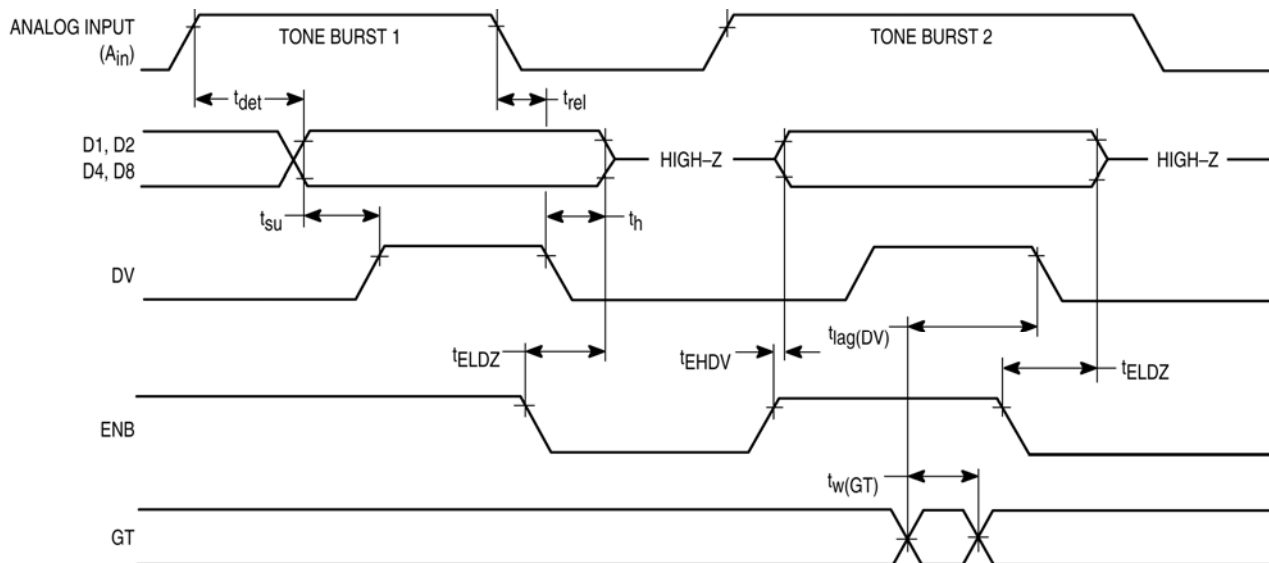


Fig. 1

Electrical DC Characteristics

($V_{DD}=5.0\pm 10\%$; $T_A=-40$ to $85\text{ }^\circ\text{C}$; Unless otherwise noted)

Parameter	Min	Typ	Max	Unit
Signal level detection	-35	-	-2	dBm
Twist = High Tone/ Low Tone	-10	-	10	dB
Frequency Detect Bandwidth	$\pm(1.5+2\text{Hz})$	± 2.5	± 3.5	$\%f_0$
50 Hz Tolerance	-	-	0.8	V_{rms}
Dial Tone Tolerance (Referenced to lower Amplitude Tone) (Dial Tone 330 + 440)	-	-	0	dB
Noise Tolerance (Referenced to lower Amplitude Tone & Bandwidth limited [0 to 3.4]kHz; Gaussian Noise)	-	-	-12	dB
Power Supply Noise (Wide Band)	-	-	10	mV p-p
Talk off (Mitel Tape #CM7290)	-	2	-	Hits

Table 2

All polarities Referenced to $V_{SS}=0[V]$; $V_{DD}=5\pm 10\%[V]$; $T_A=-40$ to $85\text{ }^\circ\text{C}$, Unless otherwise noted!

Parameter	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	V_{DD}	3	5	5.5	V
Supply Current ($f_{CLK}=3.58\text{MHz}$)	I_{DD}	-	5	8	mA
Input Voltage Low ENB, GT, X_{en}	V_{IL}	-	-	1.5	V
Input Voltage High ENB, GT, X_{en}	V_{IH}	3.5	-	-	V
I_{out} Data and DV Pins; $V_{out}=4.5[V]$ (Source)	I_{OH}	800	-	-	μA
I_{out} Data and DV Pins; $V_{out}=0.4[V]$ (Sink)	I_{OL}	1.0	-	-	mA
Input Impedance A_{in}	R_{in}	90	100	-	$\text{k}\Omega$
Fanout ATB	F_{OUT}	-	-	10	
Input Capacitance V_{en}, ENB	C_{in}	-	6	-	pF

Pin Description

V_{DD}
Positive Power Supply
(PDIP, SOG – Pin 4)

The digital supply pin, which is connected to the positive side of the power supply.

V_{SS}
Ground
(PDIP – Pin 8, SOG – Pin 9)

Ground return pin typically connected to the system ground.

$D1, D2, D4, D8$
Data Output
(PDIP – Pins 2, 1, 14, 13; SOG – Pins 2, 1, 16, 15)

These digital outputs provide the hexadecimal codes corresponding to the detected digit. The digital outputs become valid after a tone pair has been detected and are cleared when a valid pause is timed. See Table 1 for hexadecimal codes. These output pins are high impedance when the enable pin is at logic 0.

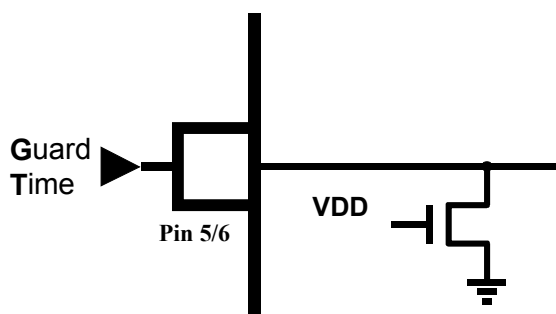
ENB
Enable
(PDIP, SOG — Pin 3)

Outputs D1, D2, D4, D8 are enabled when ENB is at a logic 1, and high impedance (disabled) when ENB is at a logic 0.

GT
Guard Time
(PDIP — Pin 5, SOG — Pin 6)

The guard time control input provides two sets of detected time and release time, both within the allowed ranges of tone on and tone off (see Figure 2). A longer tone detects time rejects signals too short to be considered valid. With GT = 1, talk off performance is improved, since it reduces the probability that tones simulated by speech will maintain signal conditions long enough to be accepted. In addition, a shorter release time reduces the probability that a pause simulated by an interrupt in speech will be detected as a valid pause. On the other hand, a shorter tone detect time with a long release time would be appropriate for an extremely noisy environment where fast acquisition time and immunity to dropouts would be required. In general, the tone signal time generated by a telephone is 100 ms, nominal, followed by a pause of about 100 ms. A high-to-low or low-to-high transition on the GT pin resets the internal logic and the SW136 is immediately ready to accept a new tone input. If left open, this pin is internally pulled to ground.

Fig.2



X en
Oscillator Enable
(PDIP — Pin 6, SOG — Pin 7)

A logic 1 on X en enables the on-chip crystal oscillator. When using alternate time base from the ATB pin, X en should be tied to VSS.

A_{IN}
Analog input
(PDIP – Pin 7, SOG – Pin 8)

The analog input is the signal-input pin for the devices, and is specially biased to facilitate its connection to external circuitry, as shown in Figure 3. The signal level at the analog input pin must not exceed the positive supply as stated on the device data sheets. If this condition cannot be guaranteed by the external circuitry, the signal must be AC coupled into the chip with a $0.01\mu\text{F}\pm 20\%$ capacitor.

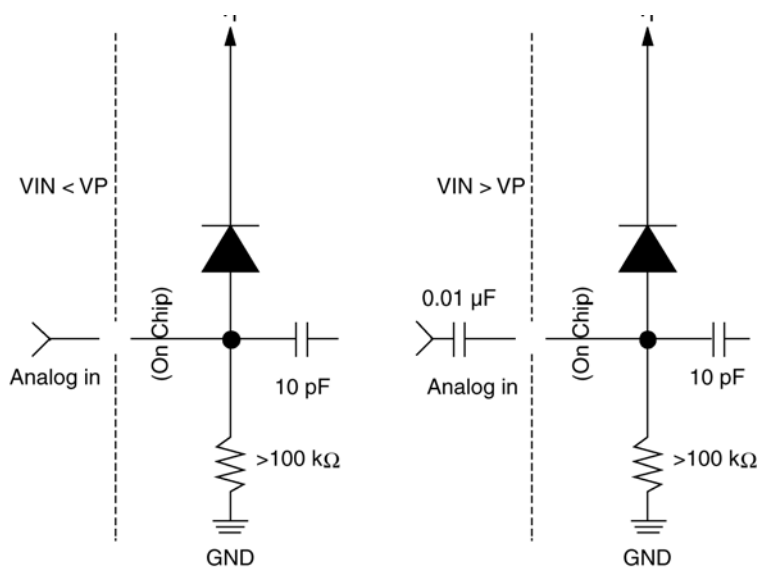


Fig. 3

X in / X out
Oscillator In and Oscillator Out
(PDIP — Pins 10, 9; SOG — Pins 11, 10)

These pins connect to an internal crystal oscillator. In operation, a parallel resonant crystal is connected from X in to X out, as well as a 1 MW resistor in parallel with the crystal. When using the alternate clock source from ATB, X in should be tied to VDD.

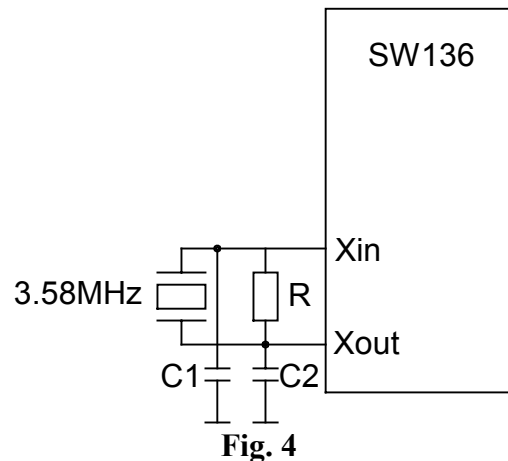


Fig. 4

ATB
Alternate Time Base
(PDIP — Pin 11, SOG — Pin 12)

This pin serves as a frequency reference when more than one SW136 is used, so that only one crystal is required for multiple SW136's. When doing so, all ATB pins should be tied together as shown in Figure 4. When only one SW136 is used, this pin should be left unconnected. The output frequency of ATB is 447.4 kHz.

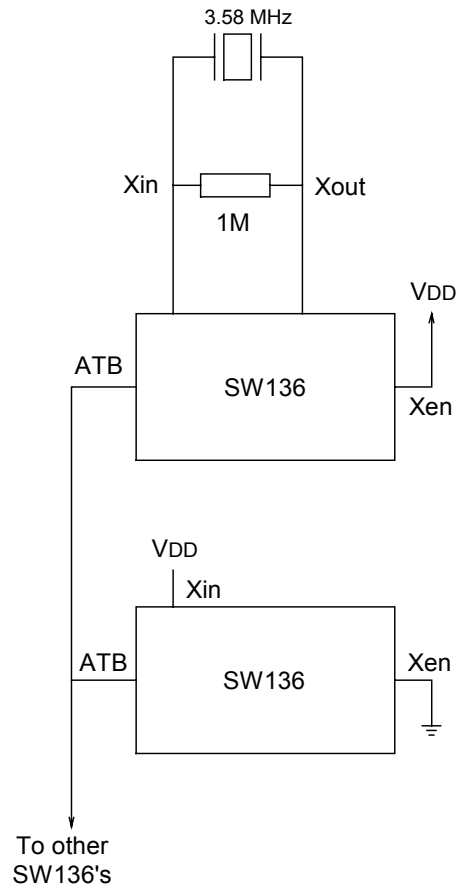


Fig. 5

DV
Data Valid
(PDIP — Pin 12, SOG — Pin 14)

DV signals a detection by going high after a valid tone pair is sensed and decoded at output pins D1, D2, D4, D8. DV remains high until a loss of the current DTMF signal occurs or until a transition in GT occurs.

Pin number		Pin Name	Description
DIP	SOC *		
1	1	D2	Data Output
2	2	D1	Data Output
3	3	ENB	Enable output
4	4	VDD	High Power Supply
5	6	GT	Guard Time
6	7	Xen	Oscillator Enable
7	8	Ain	Analogue Input
8	9	GND	Low power Supply
9	10	Xout	Oscillator Out
10	11	Xin	Oscillator In
11	12	ATB	Alternate Time Base
12	14	DV	Data Valid
13	15	D8	Data Output
14	16	D4	Data Output

Note: (*) SOC pins 5 and 13 are not connected

Pin configuration:

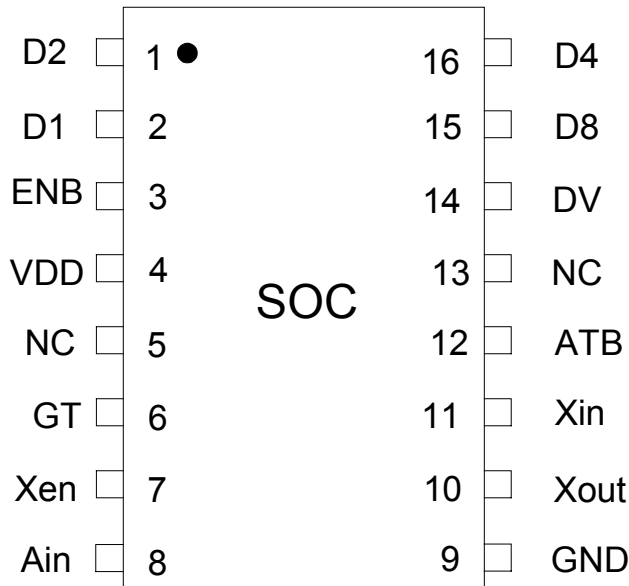
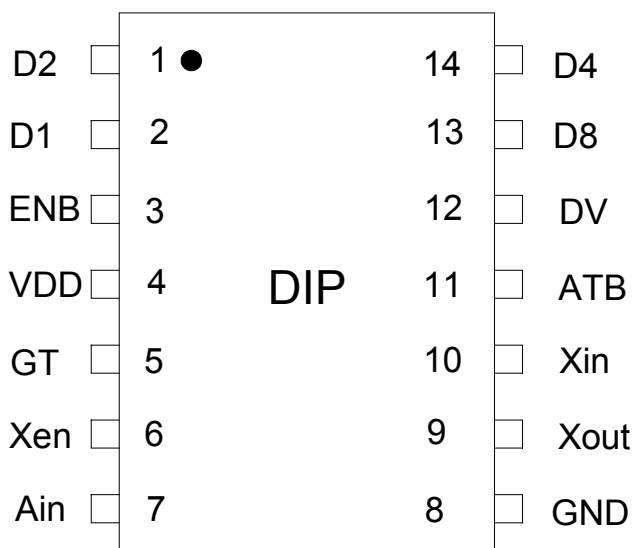


Fig. 6

