ID MOS

SW161

High data-rate
433 MHz Receiver

DATA SHEET

Typical Applications

- ➔ Wireless data link
- ➔ Wireless security systems
- ➔ Remote control
- ➔ Remote sensing

Features

- ➔ Fully Monolithic Integrated Receiver.
- ➔ No RF external components .
- ➔ Support the European 433MHz ISM band.
- ➔ Support Digital ASK, FSK modulations.
- ➔ High sensitivity: -108dBm
- ➔ High Data Rate up to 128 kbps.
- ➔ Internal PLL Frequency Synthesizer.
- ➔ Designed to allow Multi Channel operation mode.
- ➔ Dynamic configuration control
- ➔ Tunning channel down to 25 kHz step.
- ➔ High blocking immunity
- ➔ Single 2.7 – 3.3V power Supply with Power Down.

Product Description

SW161 is a fully integrated receiver circuit, designed for low to high data-rate wireless links or for secure radio communications. Operating in the European 433 MHz ISM band, it is intended for digital (ASK, FSK) modulations. SW161 is a widely configurable device which includes two internal local oscillators allowing multi - channel capabilities for complete and efficient use of the ISM band. A convenient digital serial port provides dynamic device configuration for accurate channel shift and smart consumption management. Together with ID MOS's SW220, it comes as a complementary part for fully integrated ISM receivers.

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1 Product Overview

1.1 SW161 description.

The SW161 is a monolithic receiver circuit.
It is designed for low to high data rate wireless links or for secured radio communications operated in the European 433 MHz ISM band.
The device includes a dual I/Q receiver chain to reduce antenna filtering constraint.
It is intended for digital (ASK, FSK) modulations.
It integrates an on-chip high frequency local oscillator based on a fully integrated frequency synthesizer only requiring an external crystal.
Channel selection is performed by the second integrated mixer of which second fully internal local oscillator synthesizer allows Multi channel capability.

The receiving path incorporates a LNA, two mixers and integrated filters.
All gain stages are level controlled, to achieve the best sensitivity (-108 dBm typical) in reception while avoiding front-end saturation.
The gain is auto controlled.
Base band filtering uses an external 10.7 MHz ceramic filter.
The user can choose adequate baseband bandwidth and fix maximum gain sensitivity of SW161.
The SW161 includes a digital serial interface for dynamic power management configuration and channel selection.

1.2 Operating principles

SW161 is built around a weaver architecture to provide a good image frequency rejection, a large dynamic range and blocking immunity.

High sensitivity is ensured by a low-noise input amplifier.
The circuit contains two mixers and an I/Q chain. The first mixer is built around a fixed-frequency local oscillator; the second one uses a programmable PLL synthesizer. Channel selection is performed by this second oscillator.

The user selects the channel by writing appropriate data in the digital serial interface.

The I/Q chains rejects the first frequency images; on each branch (I&Q), a fully integrated filter rejects the second frequency images.

The user defines the channel bandwidth by choosing the adequate 10.7 MHz ceramic external filters.

Variable gain amplifiers allow a good signal-to-noise ratio and provide the demodulator with the right signal level.

1.3 *Functional and Block diagram of SW161*

SW161 is the core of the 433 MHz receiver.

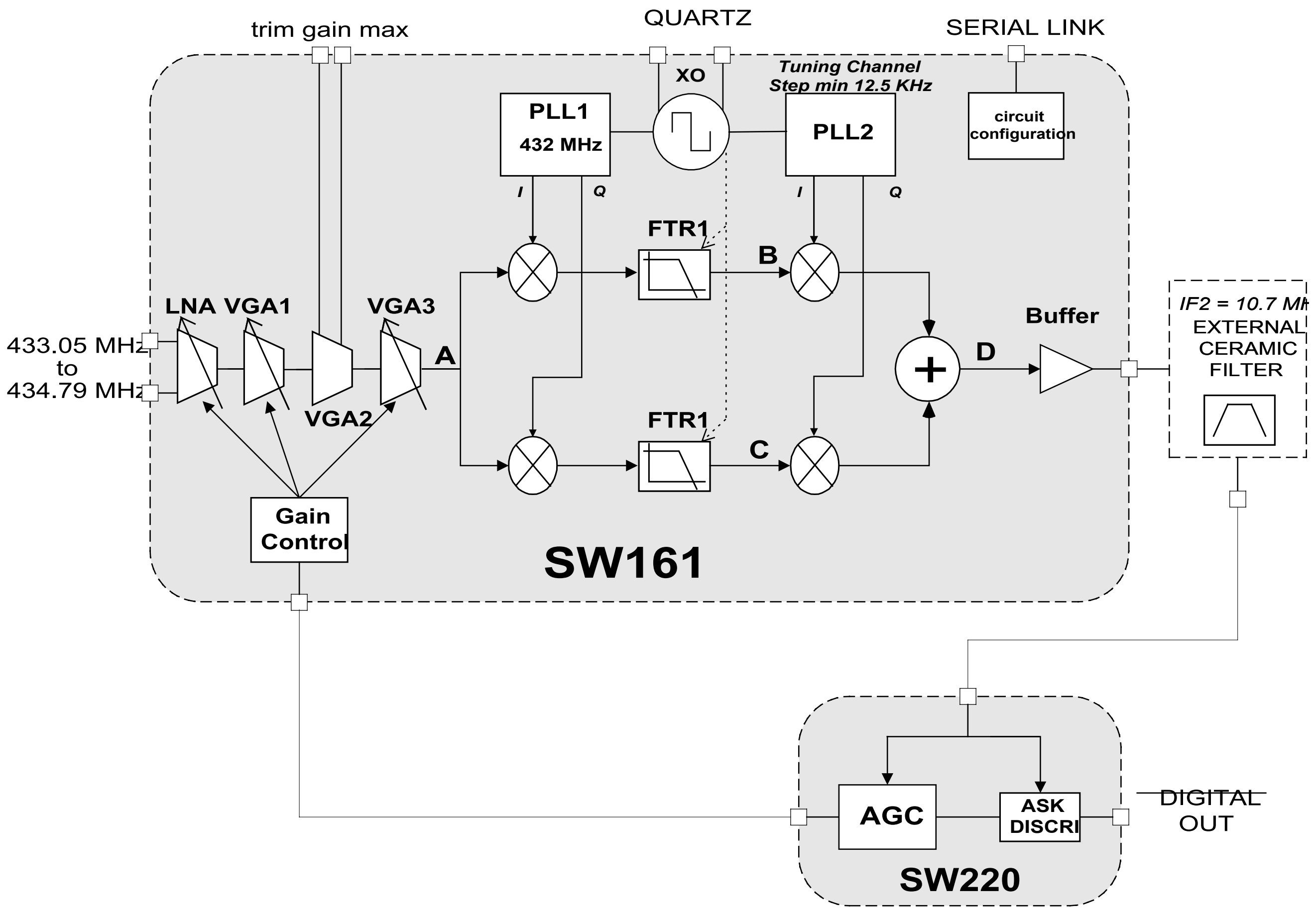
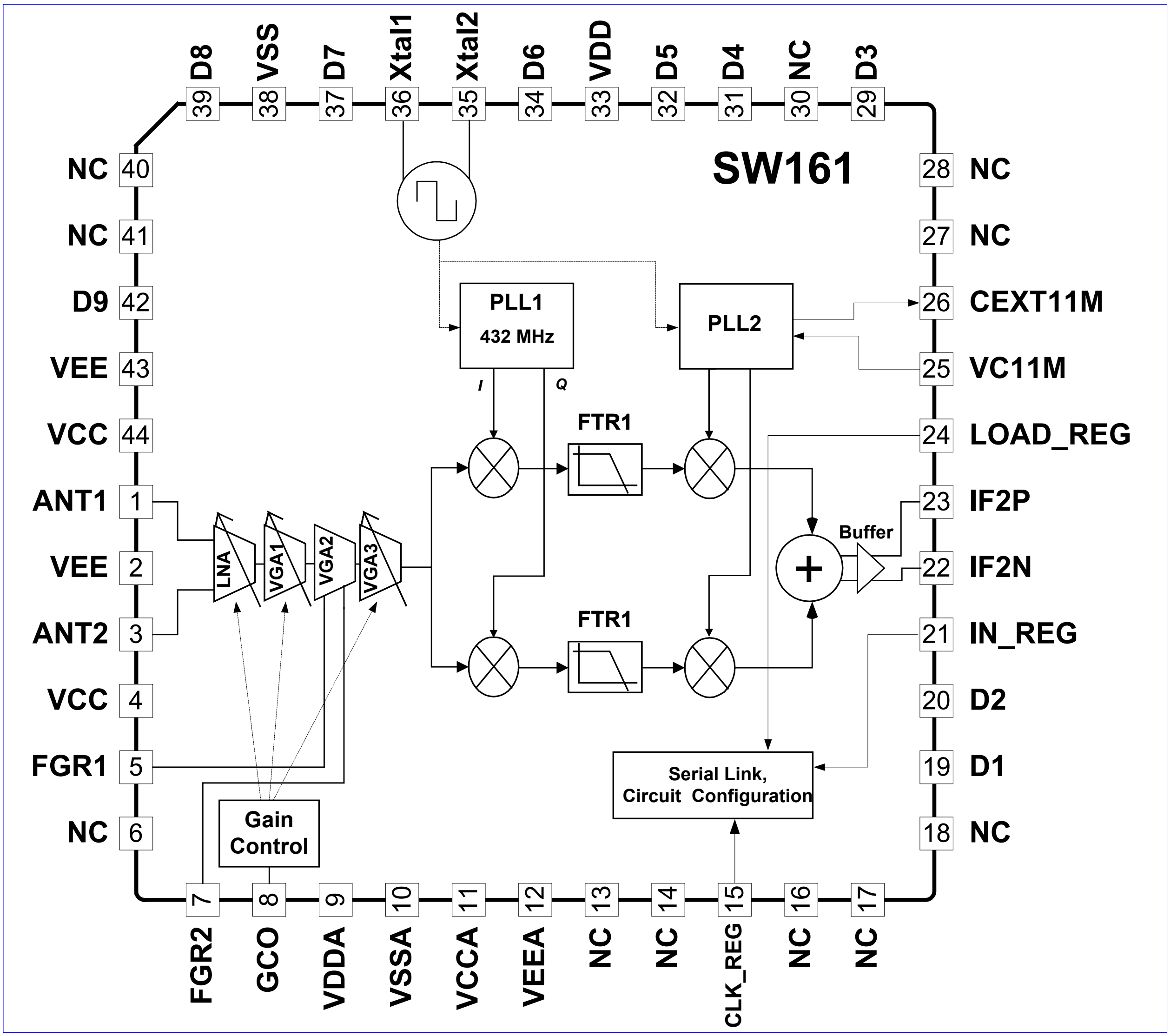


Fig. 1 : Functionnal diagram

List of main blocks used inside SW161:

Blocks	Function
LNA	Low Noise Amplifier
VGA1,VGA2,VGA3	Variable Gain Amplifier
FTR1	Lowpass filter
PLL1	first local oscillator
PLL2	second local oscillator synthesizer

Bloc diagram:



1.4 *I/O Description*

1.4.1 Operating pads

Name	Pin	Type	Function
ANT1	1	Input RF	Antenna
VEE	2	Power	Analog Ground
ANT2	3	Input RF	Antenna
VCC	4	Power	Analog power
FGR1	5	Analog i/o	VGA2 – gain adjustment
FGR2	7	Analog i/o	VGA2 – gain adjustment
GCO	8	Analog i/o	Automatic Gain Control Input
VDDA	9	Power	Analog power
VSSA	10	Power	Analog Ground
VCCA	11	Power	Analog power
VEEA	12	Power	Analog Ground
CLK_REG	15	Digital Input *Input CMOS buffer*	Shift register clock to load serial configuration data's input
IN_REG	21	Digital Input *Input CMOS buffer*	Data shift register input
IF2N	22	Analog i/o	Output IF2 differential (negative)
IF2P	23	Analog i/o	Output IF2 differential (positive)
LOAD_REG	24	Digital Input *Input CMOS buffer*	Clock to load data from shift register into load register
VC11M	25	Analog i/o	Voltage control of oscillator
CEXT11M	26	Analog i/o	PLL loop filter
VDD	33	Power	Digital Power
Xtal2	35	Analog i/o	Crystal Oscillator – External Quartz 12 MHz
Xtal1	36	Analog i/o	Crystal Oscillator – External Quartz 12 MHz
VSS	38	Power	Digital Ground
VEE	43	Power	Analog Ground
VCC	44	Power	Analog power

1.4.2 Dedicated pads

All following pads are dedicated. They shall remain UNCONNECTED at any time.

Name	Pin	Type
D1	19	Dedicated pin
D2	20	Dedicated pin
D3	29	Dedicated pin
D4	31	Dedicated pin
D5	32	Dedicated pin
D6	34	Dedicated pin
D7	37	Dedicated pin
D8	39	Dedicated pin
D9	42	Dedicated pin

2 Device characteristics

2.1 *Absolute maximum ratings*

Maximum ratings are the extreme limits to which the device can be exposed without permanent damages. It is not guaranteed to operate properly at the maximum ratings. Refer to next chapter for guaranteed conditions.

Parameter	Min	Max	Unit	Note
Supply voltage	-0.5	7	V	1)
Storage temperature	-55	125	°C	
electrostatic discharge (ESD)		1000	V	2)

1) Exposure to absolute maximum rating conditions for extended periods may affect device reliability (e.g hot carrier degradation).

2) According to MIL STD 883C, method 3015.7 .

2.2 *Operating conditions*

Parameter	Min	Typ	Max	Unit
Operating free-air temperature	-20	25	+80	°C
Supply voltage	2.7	3	3.3	V
Supply current in active mode		24		mA
Supply current Power down mode		<0,5		µA

All parameters given in the following sections are only valid up on respect to those operating conditions.

2.3 *Electrical AC characteristics*

(T_A = 25 °C, V_{CC} = 3 V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Frequency Range	FR		433.05 – 434.79			MHz	1
Digital frequency tuning step	N	For all frequency range 433.05-434.79 MHz For ½ frequency range 433.05-434 MHz	-	25 12.5	-	KHz KHz	
Channel Bandwidth	CBW	Fixed by ceramic 10.7 MHz Bandwith	-	-	580	KHz	
Modulation Scheme	MS	Discriminator option.	Non-coherent ASK or Non-coherent FSK			- -	
Data Rate	DR	ASK	-	-	128	Kbps	
Sensitivity	S_{RF}	ASK, BER = 1%, RF load = 50 Ω modulation index m=1	-108	-	-	dBm	2
Co-Channel Rejection	CR	depending on 10.7 MHz filter		40		dB	
Blocking Immunity	BI			40		dB	
Maximum Receiver Input Level	ILMAX	1 channel, BER = 1%		-15		dBm	
Antenna Port Impedance	Z_A	433.92 MHz	-	50	-	Ω	
First Local Oscillator Frequency	f_{LO1}		-	432	-	MHz	
Second Local Oscillator. Frequency	f_{LO2}	25 KHz step	7	12.6	15	MHz	
Second Local Oscillator. Frequency	f_{LO2}	12.5 KHz step	7	12.2	12.7	MHz	
Receiver Wake Up Time	t_{WR}	Cold Start		3		ms	

Note (1): This frequency range corresponds with the 433 MHz ISM band. An 868 MHz ISM band device will be soon available.
Note (2): The calculation of the sensitivity takes only the modulated signal bandwidth into account.
Note (3): SW161 is compliant to I-ETS 300-220.

2.4 Digital bloc characteristics

2.4.1 Series to parallel shift register bloc description

The SW161 contains an interface (series to parallel shift register) to configure power management and channel selection.
This block enables to load parameters for digital and analog blocks.
The internal TR(12:0) outputs are sent to analog part, the other outputs are sent to digital part.
On each rising edge of CLK_REG, the input data IN_REG is shifted in a 25 bits shift register.
When a rising edge occurs on LOAD_REG, the data are loaded in the second registers line.
A reset (RST_LOADN) on the second line is necessary to initialize the parameters.

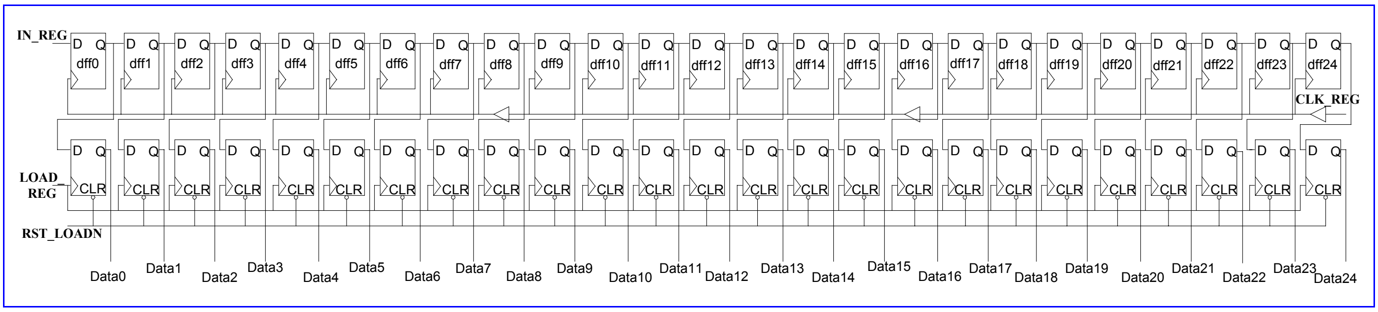


Fig. 2 : Series to parallel shift register

Pin name	pin type	Polarity	I/O synchro	function
CLK_REG	Input	0 to 1 transition		Shift register clock to load serial data's input
IN_REG	Input		YES	Data shift register input
LOAD_REG	Input	0 to 1 transition		Clock to load data from shift register into load registers
RST_LOADN	Input	0		initialize load registers

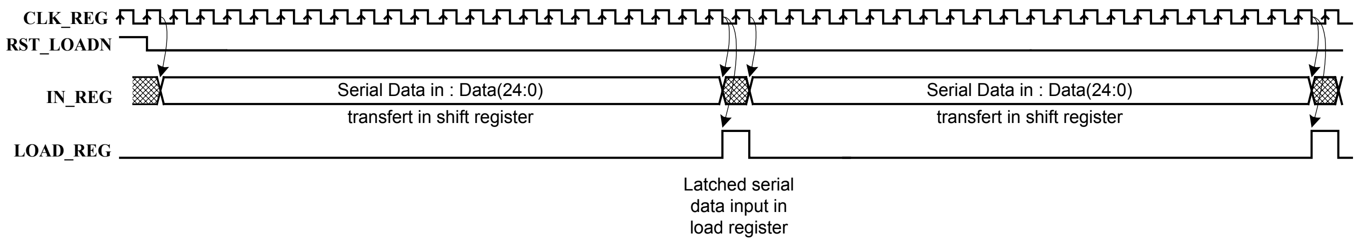


Fig. 3 : Series to parallel shift register bloc timing for load data

The Input Data are synchronizing in falling edge of CLK_REG to avoid setup and hold time problem.

2.4.2 Data configuration

Data n°	function	Value
0		must be set to 0
1	Control the low pass frequency of the integrated filter (FTR1)	Typical 1
2		Typical 0
3		Typical 0
4		Typical 0
5		Typical 1
6		Typical 0
7		Typical 0
8		Typical 0
9	control the VCO gain (K specified in MHz/V)	Typical 0
10		Typical 1
11	Power control	The circuit is OFF when Data 11 is set to 0 The circuit is ON when Data 11 is set to 1
12		must be set to 0
13		must be set to 1
14	Control the Internal Clock reference (Fclk2) of the second oscillator and the value of step	When Data14 is set to 0: Fclk2=50kHz, step=12.5kHz When Data14 is set to 1: Fclk2=100kHz, step=25kHz
15	Division value (Dv) it is coded as follow: Data(24:17): integer part Data(16:15): decimal part ➔ data(16:15)=00, decimal part = 00 ➔ data(16:15)=01, decimal part = 25 ➔ data(16:15)=10, decimal part = 50 ➔ data(16:15)=11, decimal part = 75 The frequency of the second oscillator is : f_{LO2}= Dv*Fclk2	
16		
17		
18		
19		
20		
21		
22		
23		
24		

The received frequency is fixed by setting the value of data (24:14).

<u>The received frequency F_{RF} (MHz) is:</u>

$$F_{RF} = (F_{xtal} * 36) + F_{LO2} - 10{,}7\ \text{MHz}$$
$$F_{LO2} = D_v * F_{clk2}$$

with
F_{xtal} = 12MHz
D_v : value of division, data(24:15).
Fclk2: Clock reference frequency of PLL2, data(14).

Example with Data(24:0)= 0 1111 0111 1110 1100 0010 0010:

Data (0)=0 → Imposed value
Data(8:1)= 00010001 → typical value for low pass frequency filter.
Data(10:9)=10 → typical value for VCO gain
Data(11)=1 → circuit is ON
Data(13:12)=10 → Imposed value
Data(14)=1 → Fclk2=100 kHz and step=25 kHz
Data(16:15)=11 → decimal part of Dv is 75
Data(24:17)=01111011 → integer part of Dv is 123

So,
Dv=123.75 and Fclk2=100 kHz ⇒ **F_{LO2} =12.375 MHz**

And: **F_{RF}= (12 MHz *36)+12.375 MHz – 10.7 MHz = 433.675 MHz**

3 Application notes

3.1 *Typical implementation for SW161 device.*

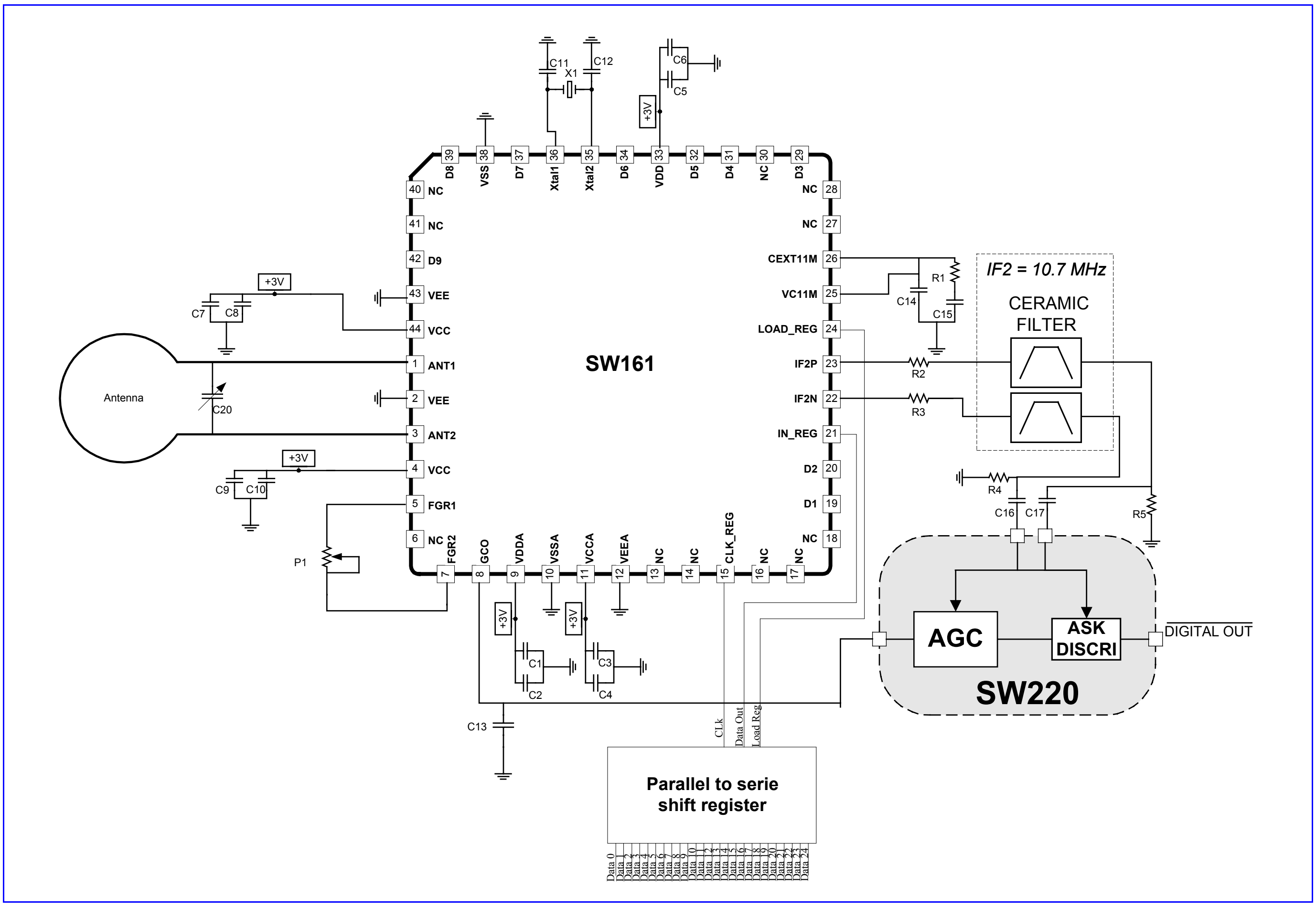


Fig. 4 : SW161 circuit connections

The value of each external components:

Component Name	Value	Unit
C1, C3, C5, C7, C9	100	nF
C2, C4, C6, C8, C10	10	pF
C11, C12	10*	pF
C13	1	µF
C14	2.2	nF
C15	22	nF
C16, C17	1	µF
C20	Adj	pF
P1	20	kΩ
R1	20	kΩ
R2, R3, R4, R5	330	Ω
X1	12	MHz
Ceramic Filter	10.7	MHz
Ceramic Filter	10.7	MHz
Parallel to series shift register		
SW220 (ASK discriminator)		

(*) according to crystal accuracy.

3.2 *PC Board Layout*

A simple glass epoxy (FR4) double face is enough for the board.
The topside of the PCB is used as ground plane. In addition there are also ground areas on the PCB's component side to ensure sufficient grounding. There are several plated contacts connecting the topside ground areas to the bottom side ground plane.
All device ground leads and bypass capacitors must be connected as close as possible to the IC package. Various technologies of capacitors for the decoupling (e.g. tantalum in parallel with ceramic) must be used. Surface mount components give better performances.
The supply lines must follow a star architecture instead of using a parallel architecture.

4 Typical measurement

The board used for typical measurement is a simple double sided glass epoxy (FR4).
The top side of the PCB is used as ground plane and the antenna does not need heavy adaptation.
The antenna is just connected through the blocking capacitor shown in figure 6.
A loop antenna adapted with device port allows some improvement of the receiver's sensitivity.

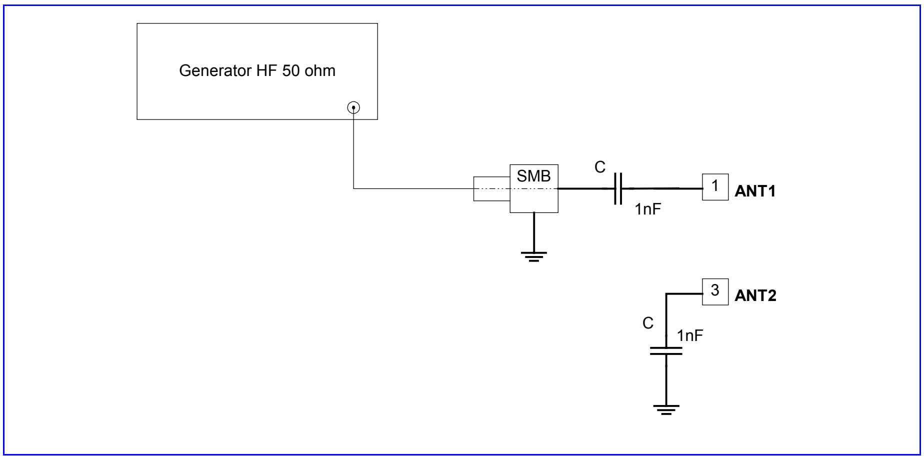


Fig. 5 : Antenna connection

Measurement configuration 1:

Generator HF:
- F_{RF}= 433.675 MHz
- level= **-108dBm**
- Modulation: AM 100%, square signal, 1kHz.

Serial interface:
- data (24:0)= 0 1111 0111 1110 1100 0010 0010

Ceramic Filter:
- murata SFE 10,7 MT
- bandwidth: 80kHz typical

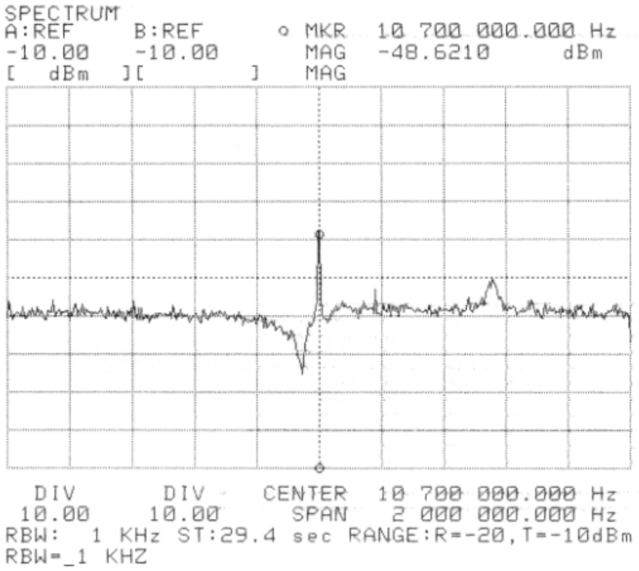


*Fig. 6 : __**Input** signal of ceramic filter (IF2P) with square modulation(1kHz), span 2Mhz__*

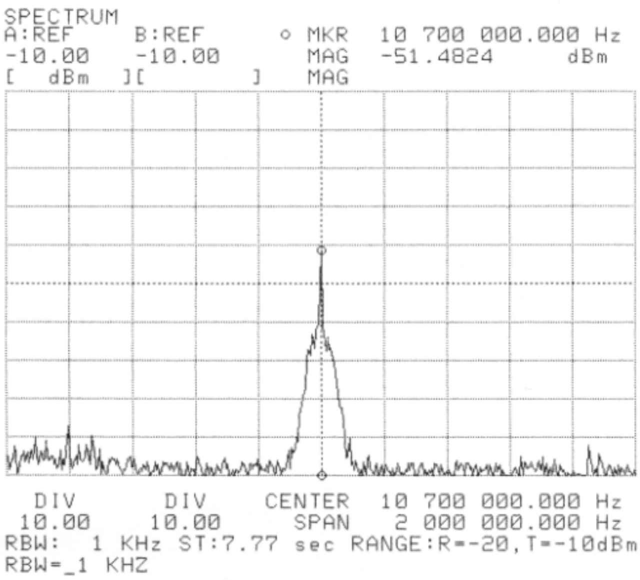


*Fig. 7 : __**Output** signal of ceramic filter (IF2P) with square modulation(1kHz), span 2Mhz__*

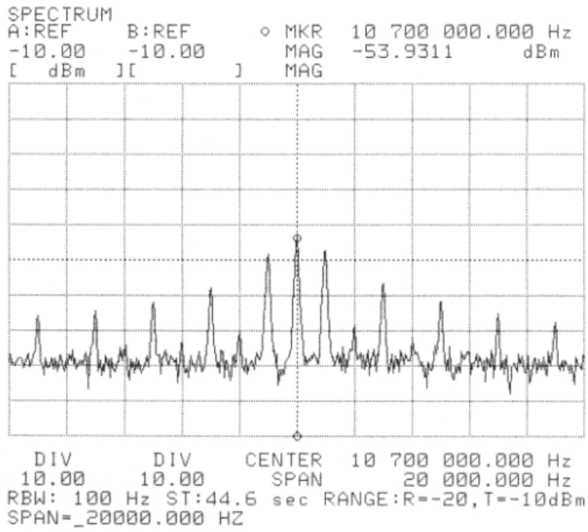


Fig. 8 : *<u>Output signal of ceramic filter **with square modulation** (1kHz), span 20 kHz</u>*

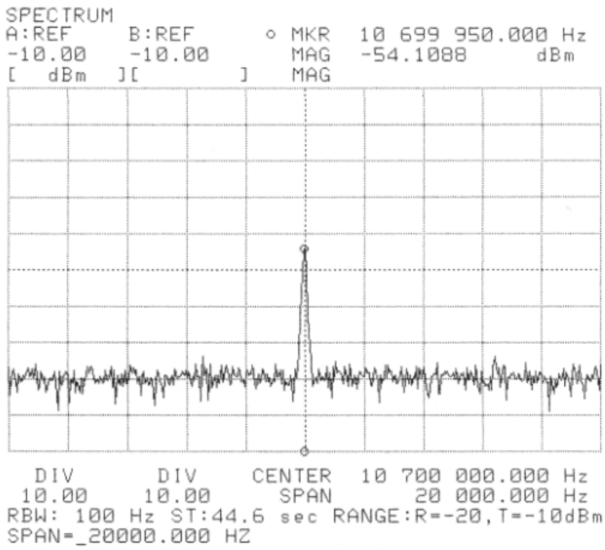


Fig. 9 : *<u>Output signal of ceramic filter **without modulation**, span 20 kHz</u>*

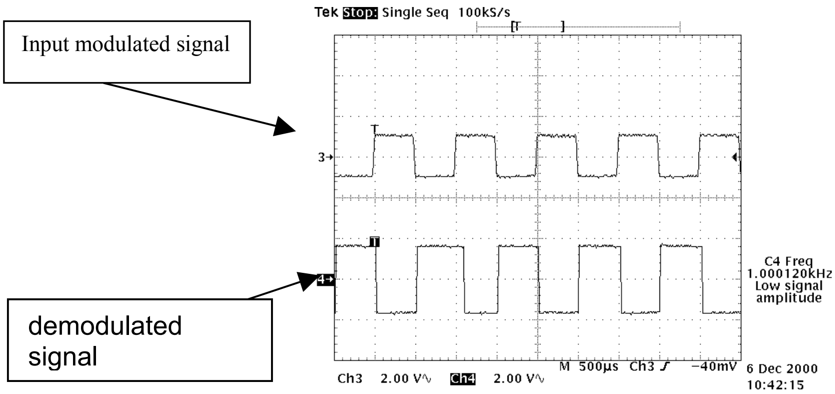


Fig. 10 :<u>Demodulated square signal 1kHz of SW220 circuit output</u>

Measurement configuration 2:

Generator HF:
- F_{RF}= 433.675 MHz
- level= **-50dBm** (AGC is working)
- Modulation: AM 100%, square or sinus signal, 1kHz.

Serial interface:
- data(24:0)= 0 1111 0111 1110 1000 0010 0010

Ceramic Filter:
- murata SFE 10,7 MT
- bandwidth: 80kHz typical

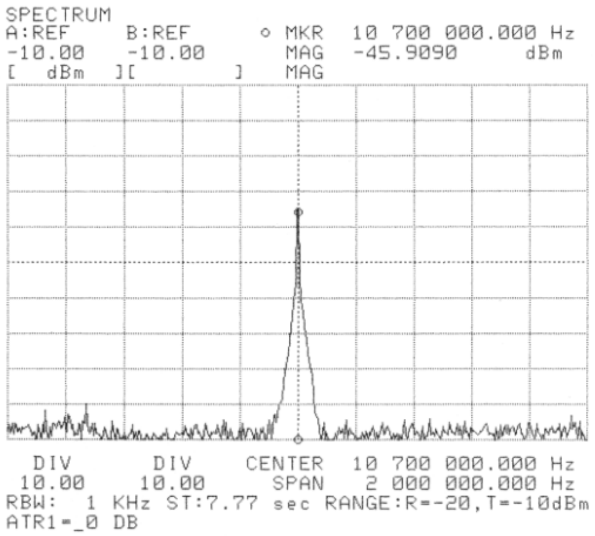


*Fig. 11 :Output signal of ceramic filter with levelHF=-50dBm, **square** signal modulation (1kHz) and span 2 MHz*

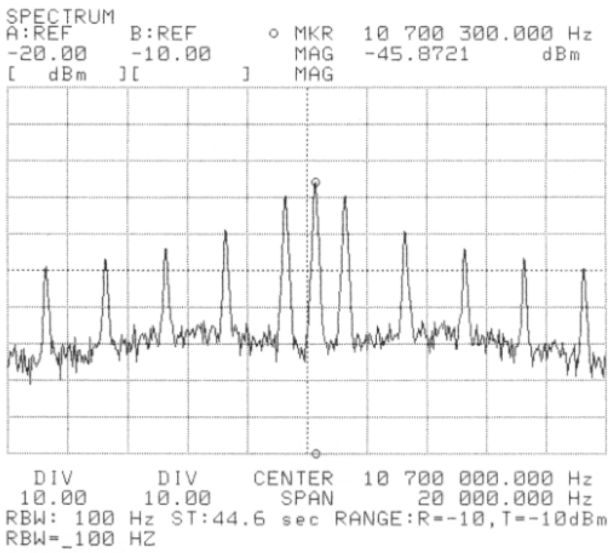


*Fig. 12 : Output signal of ceramic filter with levelHF=-50dBm, **square** signal modulation (1kHz) and span 20 kHz*

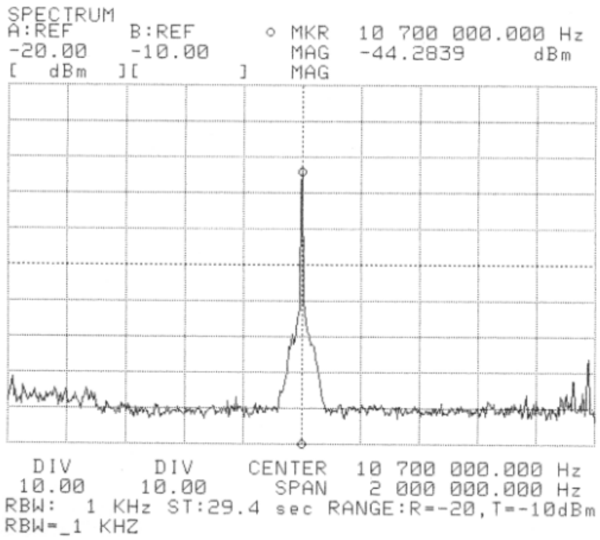


*Fig. 13 :Output signal of ceramic filter with levelHF=-50dBm, **sinus** signal modulation (1kHz) and span 2 MHz*

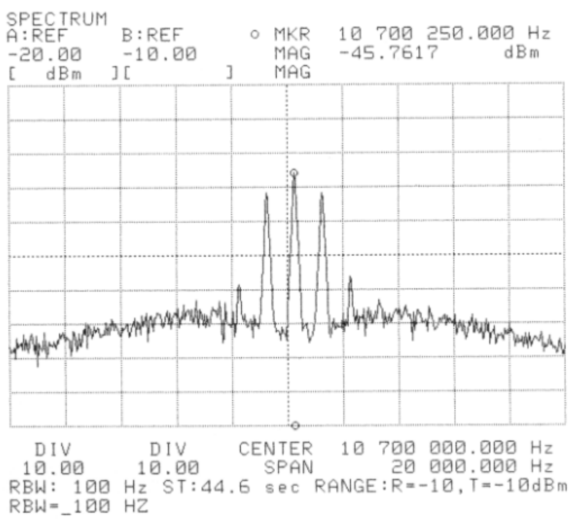


*Fig. 14 :Output signal of ceramic filter with levelHF=-50dBm, **sinus** signal modulation (1kHz) and span 20 kHz*

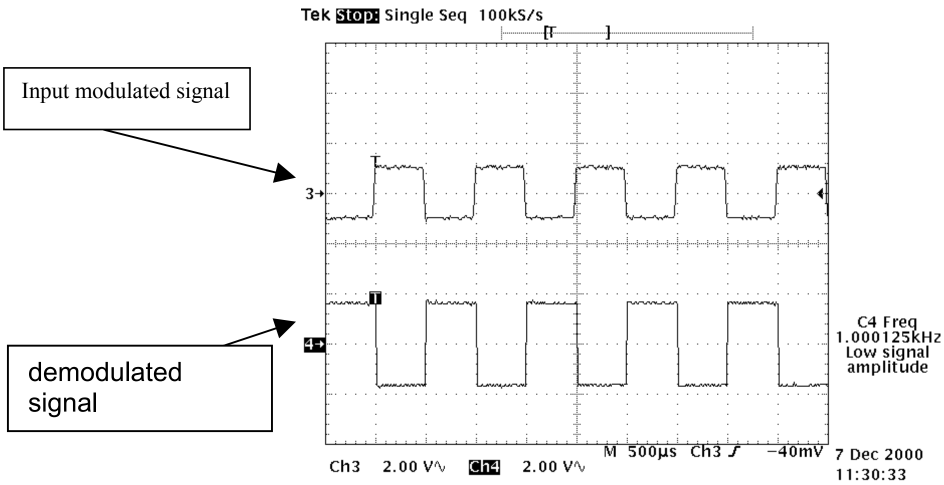


Fig. 15 :Demodulated square signal 1kHz of SW220 circuit output

5 Package outline

The SW161 is provided in a 44 pins QFP ceramic package.
The following drawing gives the product's pinout and package mecanical outlines:

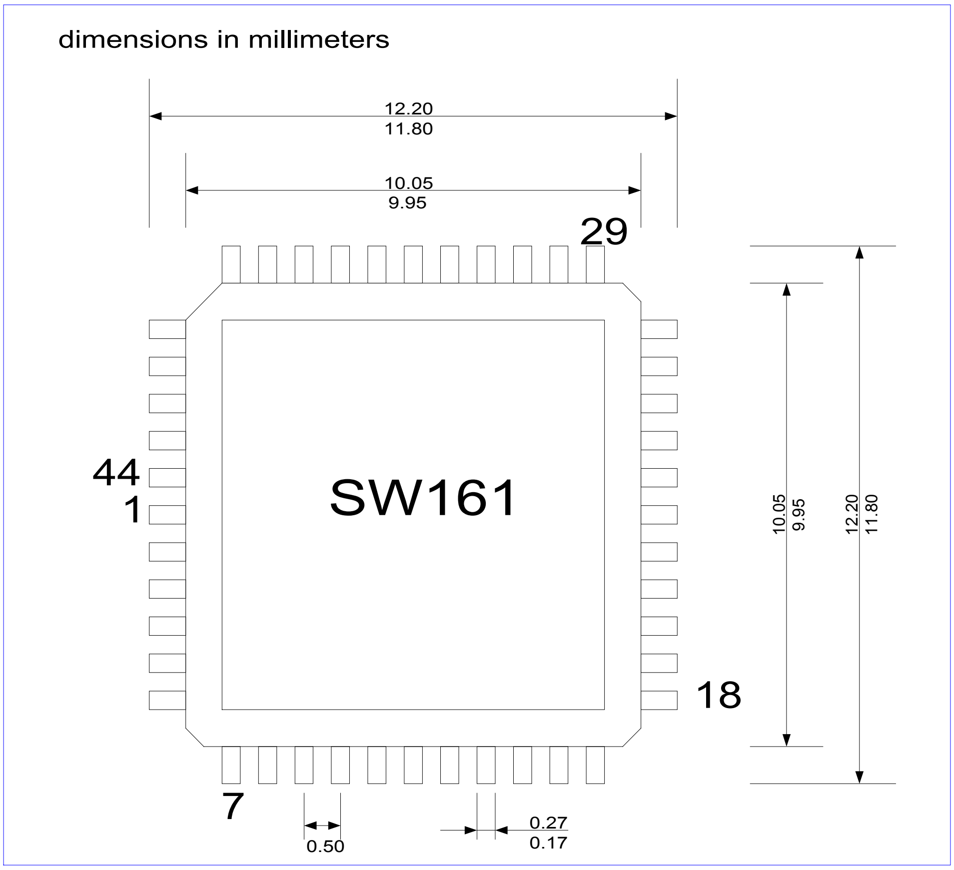


Fig. 16 :Package outline

6 Notes

The information in this data sheet is believed to be accurate and reliable. ID MOS reserves the right to make changes without prior notice to any specifications of this product. This device is not intended to be used for systems that support or sustain life or for systems where failure may cause personal injury. The customers use this product at their own risk.