

DATA SHEET

Typical Applications

- ISDN Primary Interface (PRI) (CCITT G.703)
- NIU interface to E1 Service
- E1 LAN bridge
- CPU to CPU Channel Extenders
- Digital Loop Carrier - Subscriber Carrier Systems
- E1 Multiplexer
- Channel Banks

Features

- Compliant with ITU G.703 pulse mask template
- Compliant with the EXAR XRT59L91 transceiver without the following signal pins: TXCLK, LLOOP, RLOOP AND RXLOS.
- Line impedance: 60Ω or 120Ω
- Logic inputs must accept either 3.3V or 5V level
- Low power dissipation
- Power down mode (TXPOS and TXNEG set to logic 1)
- Transformer coupling (transmit 1:2, receive 2:1)



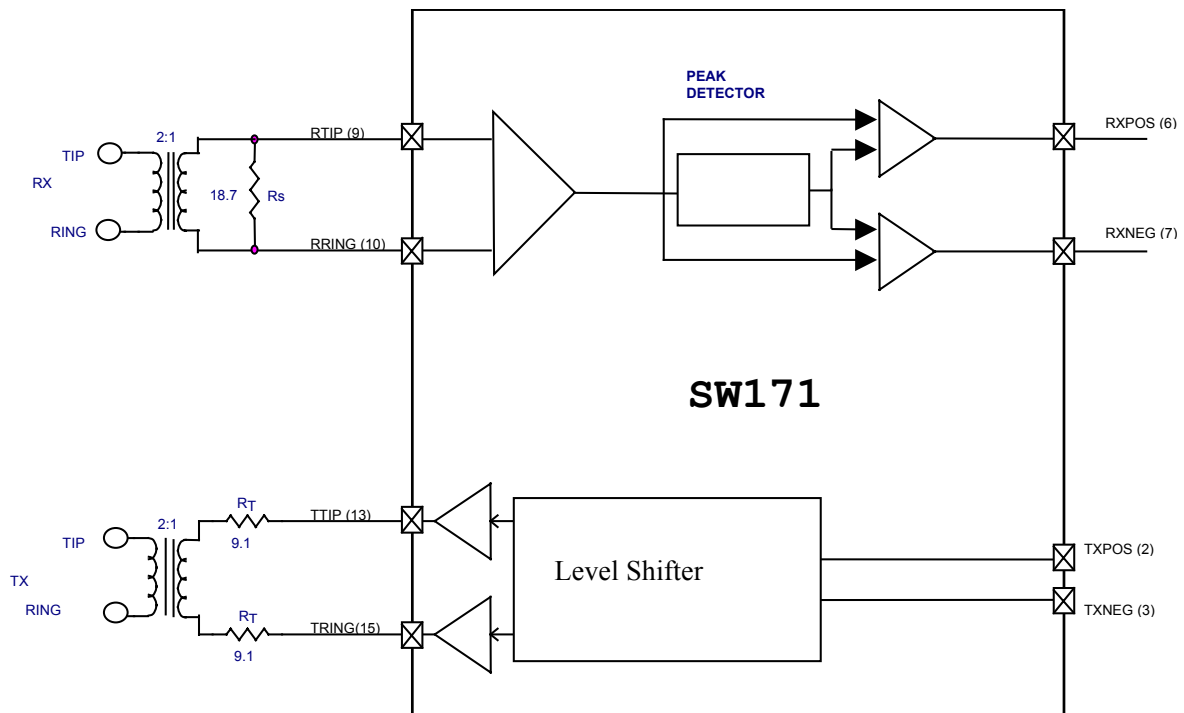
Product Description

The PAT is a purely analog bi-directional transceiver for E1 NIU and ISDN Primary Rate Interface (ISDN PRI) application at 2.048Mbps (E1). This transceiver operates over 2 km of 0.4mm twisted-pair cable without any external components.

It is built using an advanced double-poly, single-metal CMOS process and requires only a single 3.3-volt power supply.

The ID MOS PAT finds applications in widely diverse areas of telecommunication.(See above)

Functional Diagram



Absolute Maximum Ratings

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_VDD	DC Supply	-0.5		6.0	Volt	
R_VDD						
Ta	Operating Temperature	-40		+85	°C	
Tst	Storage Temperature	-65		150	°C	
ESD ratio	Human body model			2	kV	See the remark!

Remark: The company is making investigation for ESD protection at 4kV.

Electrical AC Characteristics

Transformer requirements

Input Transformer

Turn ratio	Supplier Information
1CT:2CT	Pulse PE-65861
1CT:2CT	Halo TG26-1205N1 Halo TG26-1505N1 Halo TG26-4505N1

Output Transformer

Turn ratio	Supplier Information
1CT:2CT	Pulse PE-65861
1CT:2CT	Halo TG26-1205N1 Halo TG26-1505N1 Halo TG26-4505N1

Transmitter Characteristics

AC Electrical Characteristics (Ta=-40 ÷ 85°C, VDD=3.3V ± 5%)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
T1	Transmit Data Propagation Delay Time		50		ns	
T _{XPW}	Output Pulse Width*	224	244	264	ns	
V _{TXOUT}	AMI Output Pulse Amplitude	2.7	3.0	3.3	V	120Ω application. Use transformer 1:2 with resistors in series of the primary.
	Output Pulse Width Ratio	0.95		1.05		
	Output Pulse Amplitude Ratio	0.95		1.05		
T _{Xlos}	Output Return Loss:					
	51KHz --102KHz	10			dB	
	102KHz--2048KHz	16			dB	
	2048KHz--3072KHz	12			dB	

* Refer to Figure 2 for E1 pulse mark specifications.

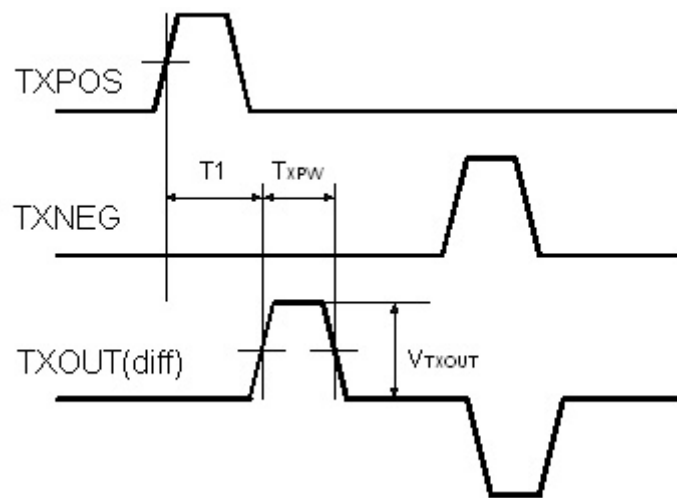


Fig.1: Transmit Data Characteristics

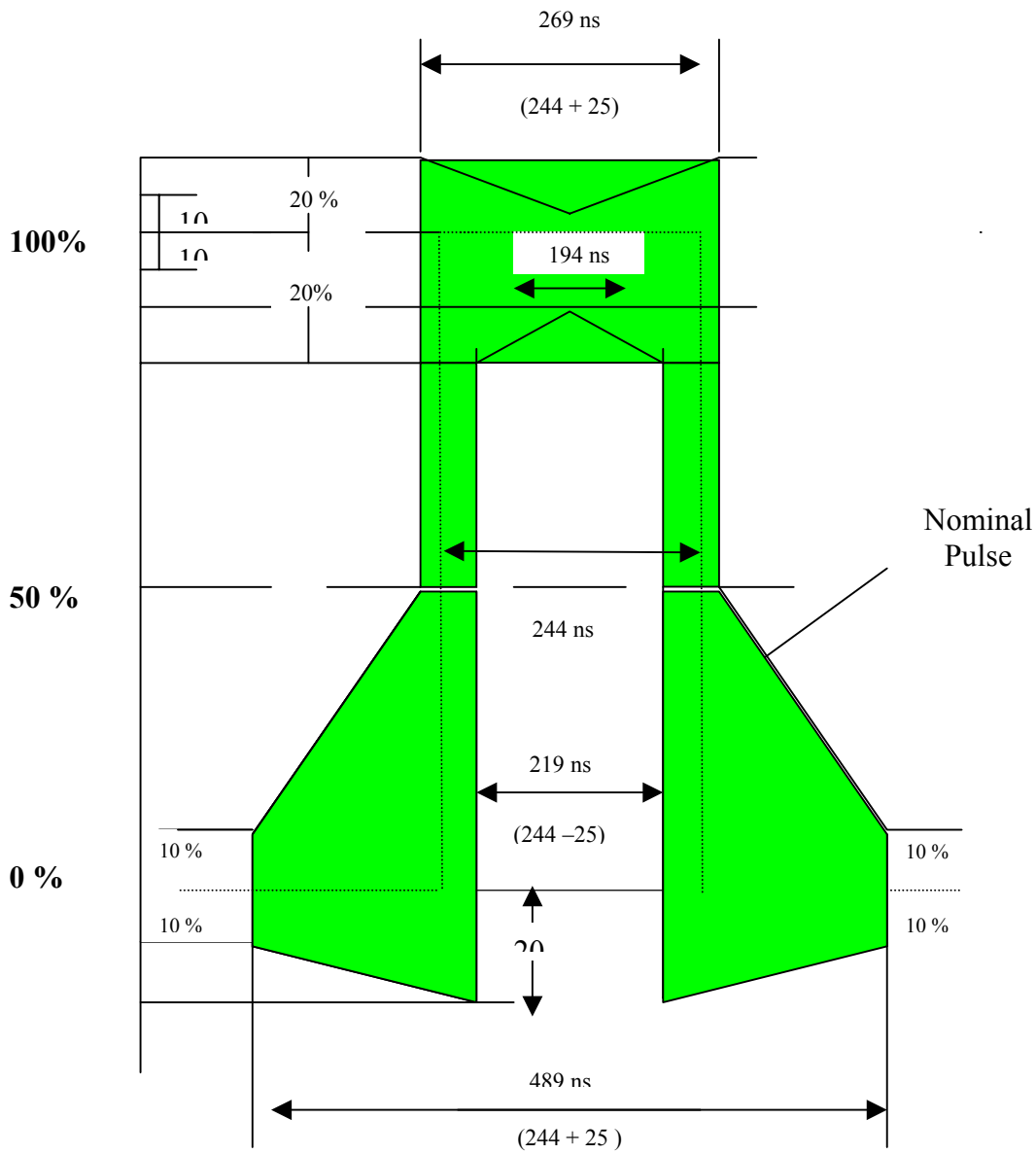


Fig.2: E1 Pulse Shape.

Parameter	Twisted Pair	Unit
Test Load Impedance	120	Ω
Nominal Peak Mark Voltage	3	Volt
Nominal Space Peak Voltage	0+/-0.3	Volt
Nominal Pulse Width	244	Ns
Ratio of positive and negative pulse amplitudes at center of pulse	95-105	%
Ratio of positive and negative pulse amplitude at nominal half amplitude	95-105	%

Receiver Characteristics

AC Electrical Characteristics (Ta=-40 ÷ 85°C, VDD=3.3V ± 5%)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
Rtr	Receive Data Rise Time			40	ns	
Rtf	Receive Data Fall Time			40	ns	
Rpd	Receive Data Propagation Delay		160		ns	
R _{xpw}	Receive Data Pulse Width	210	244	450	ns	
RXlos	Allowable Cable Loss	0	10	12	dB	Relative to 0dB=3Vpp differential
RXin	Input Impedance	5			kΩ	
RXxi	Receiver Slicing Threshold	45	50	55	%	% of peak input voltage at -3dB cable loss
RXlos	Allowable Cable Loss 51KHz --102KHz 102KHz--2048KHz 2048KHz--3072KHz	14 20 16			dB dB dB	
RXjit	Jitter Tolerance 20Hz 700Hz 10KHz-100KHz	10 5 0.3			UIpp UIpp UIpp	
TiCt	Discharge Time constant	100			ms	

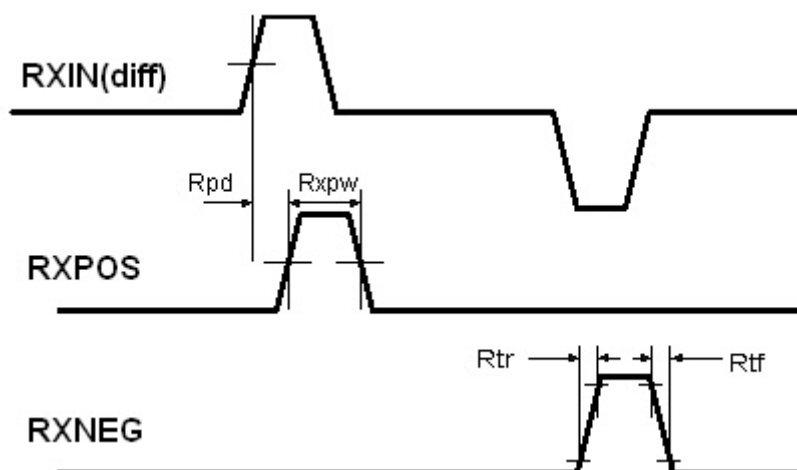


Fig. 3 Receive Time Characteristics

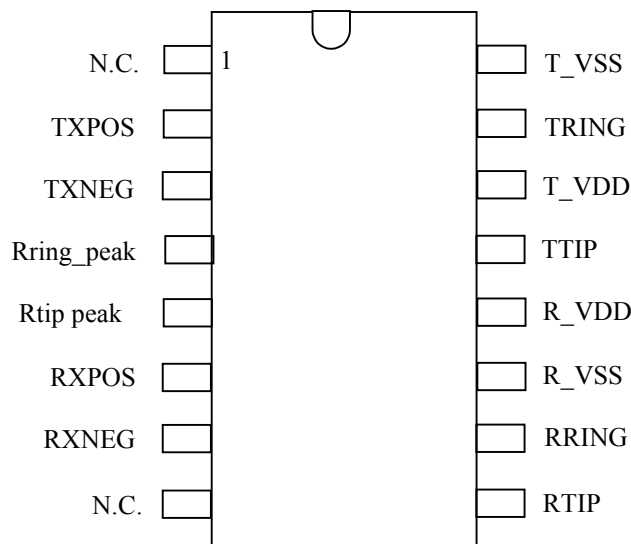
Electrical DC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_VDD R_VDD	DC Supply	3.13	3.3	3.46	Volt	
PD	Power dissipation				mW	
VIH	Input high level TxPOS, TxNEG pins	2		5	Volt	
VIL	Input Low Level TxPOS, TxNEG			0.8	Volt	
VOH	Output high level RxPOS, RxNEG	2.4			Volt	Ioh=-400uA
VOL	Output low level RxPOS, RxNEG			0.4	Volt	Iol=1.6mA
Pd	Power Dissipation			155	mW	See remark!
Ppd	Power Dissipation in Power Down Mode			30	mW	When TXPOS and TXNEG = "1"

Remark: The value is based on preliminary calculations

Pin Description

16 LD JEDEC SOIC (0.3 Inch Body)



Symbol	Pin #	I/O	Description
N.C.	1		
TxPOS	2	I	Transmitter positive data input (intern pull-up with 50 kΩ)
TxNEG	3	I	Transmitter negative data input (intern pull-up with 50 kΩ)
Rring_peak	4		Peak detector capacitance (20nF external connected to the ground)
Rtip_peak	5		Peak detector capacitance (20nF external connected to the ground)
RxPOS	6	O	Receiver positive data output. A signal on RxPOS corresponds to receipt of a positive pulse on RTIP/RRING.
RxNEG	7	O	Receiver positive data output. A signal on RxNEG corresponds to receipt of a negative pulse on RTIP/RRING.
N.C.	8		
RTIP	9	I	Receiver positive bipolar input
RRING	10	I	Receiver negative bipolar input
R_VSS	11		Receiver ground
R_VDD	12		Receiver positive supply
TTIP	13	O	Transmitter positive bipolar output
T_VDD	14		Transmitter positive supply
TRING	15	O	Transmitter negative bipolar output
T_VSS	16		Transmitter ground

